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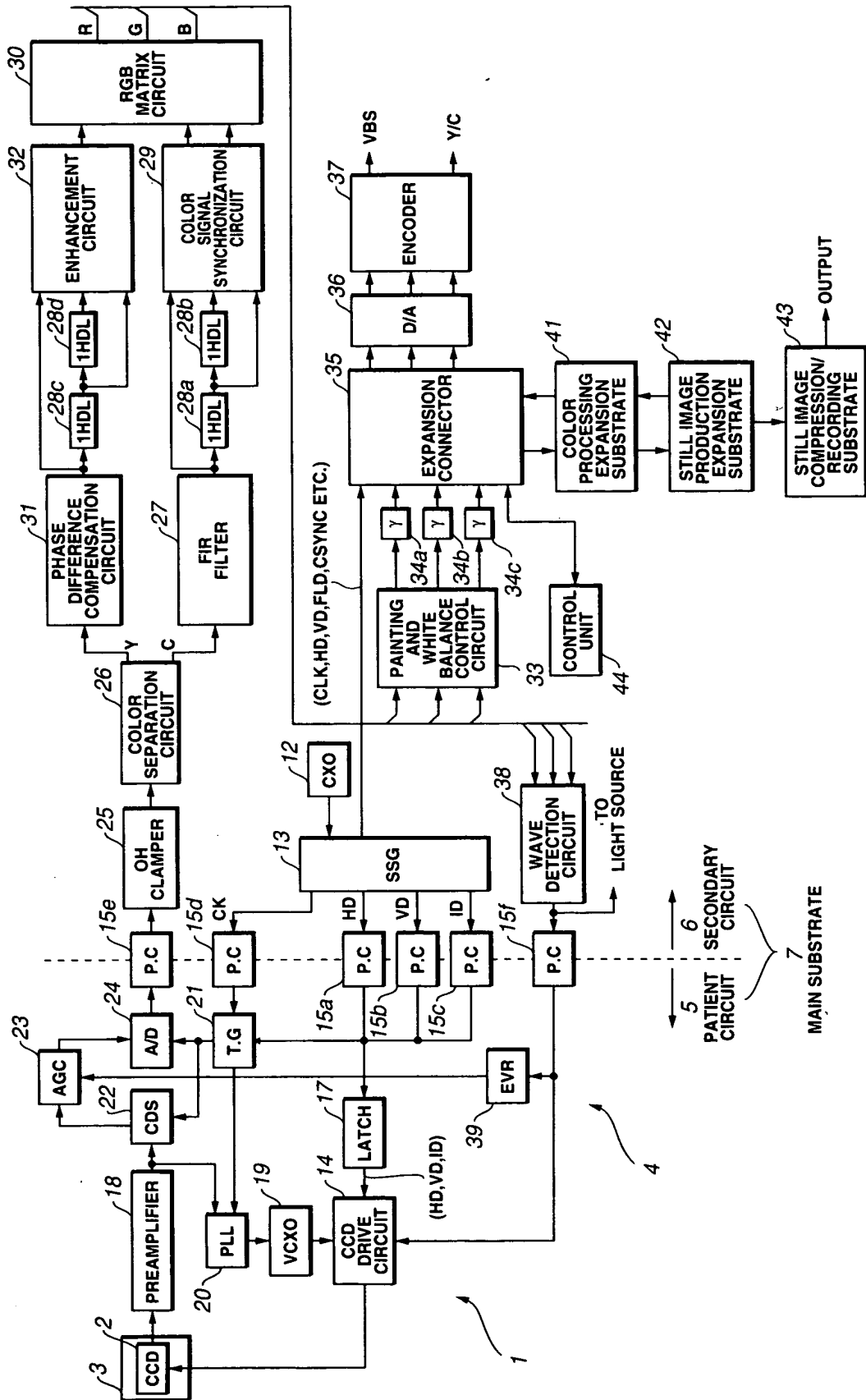
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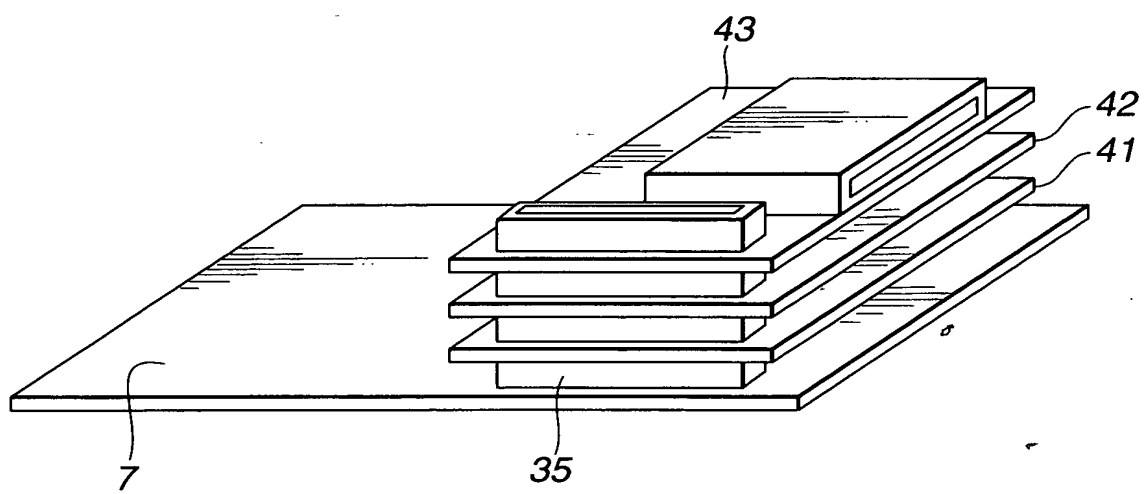
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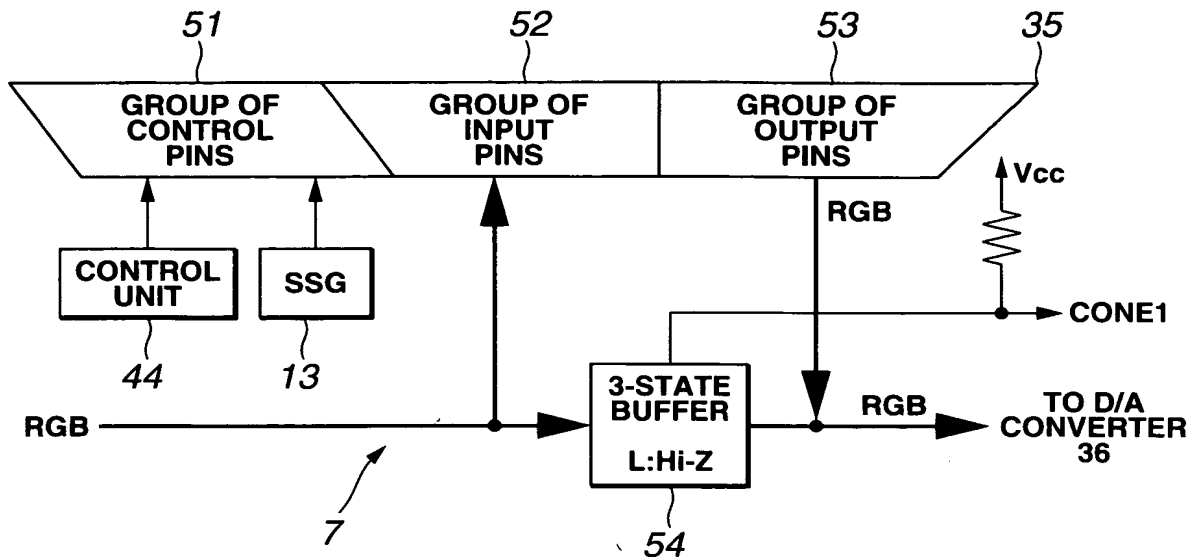
# FIG. 1



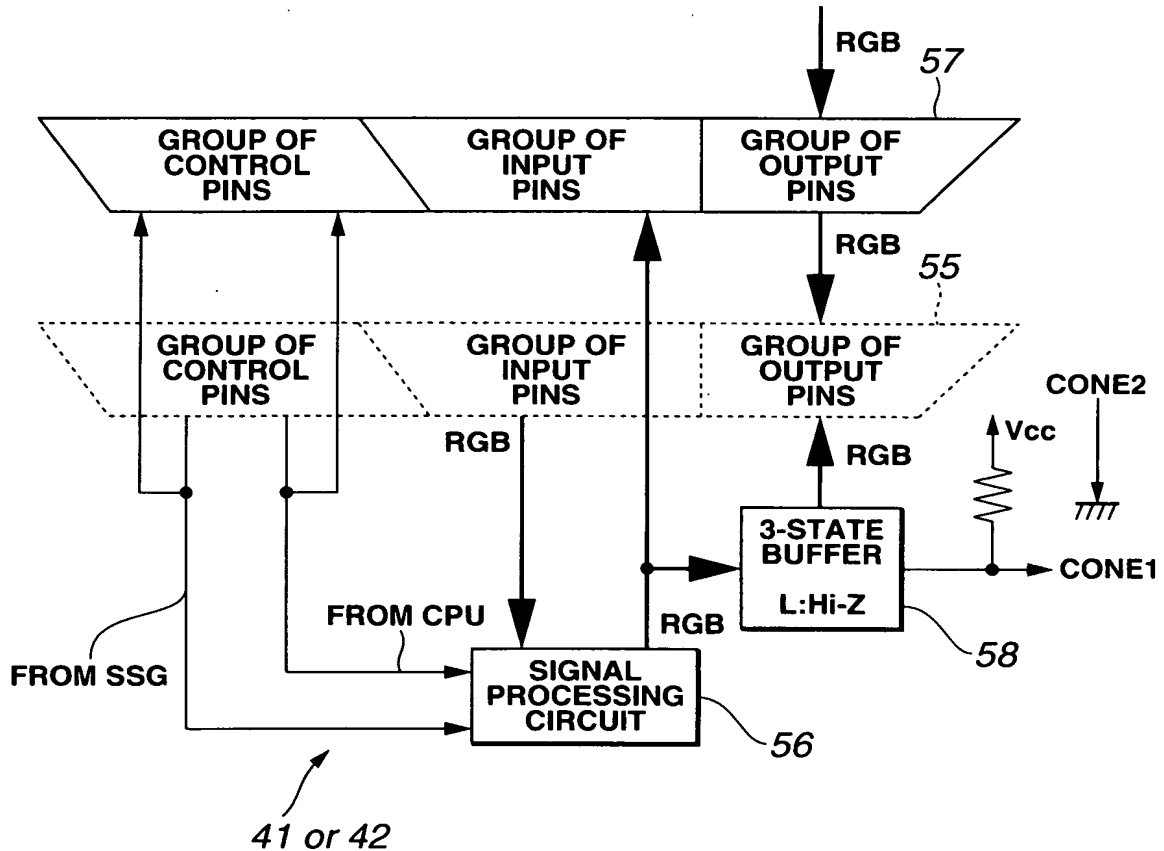
**FIG.2**



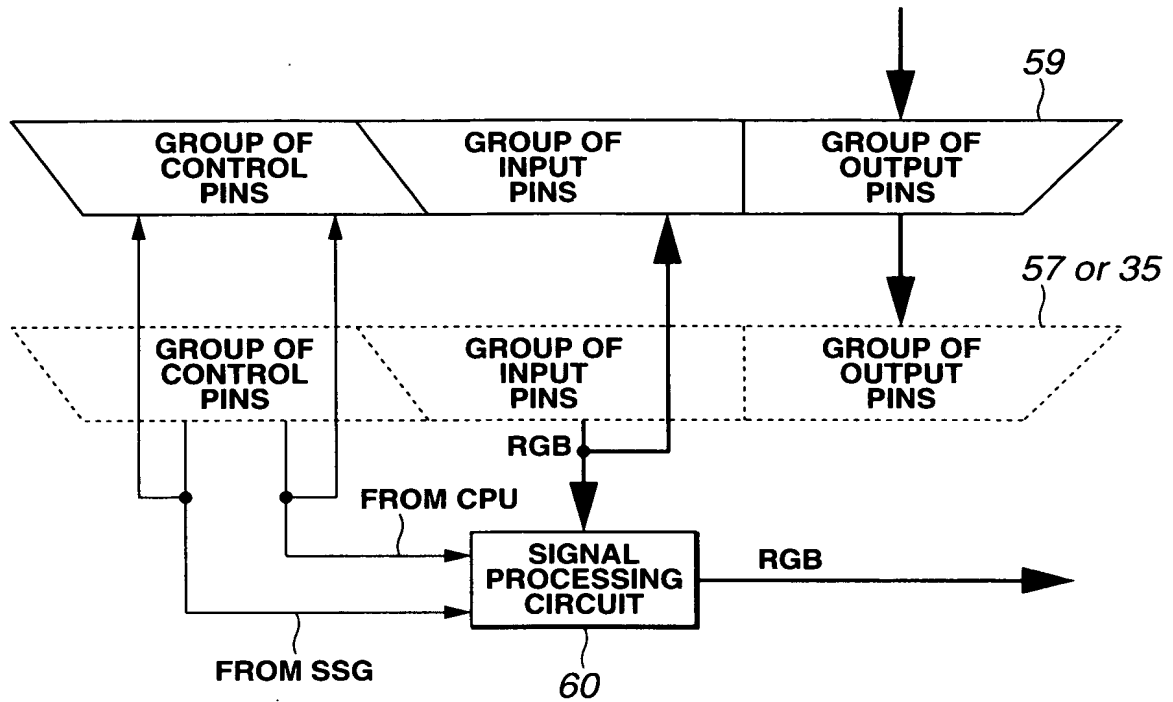
# FIG.3



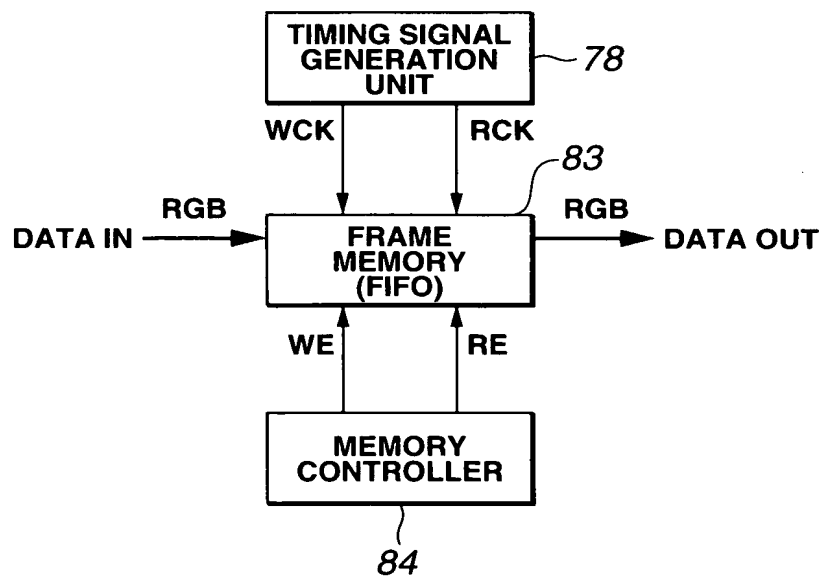
# FIG.4



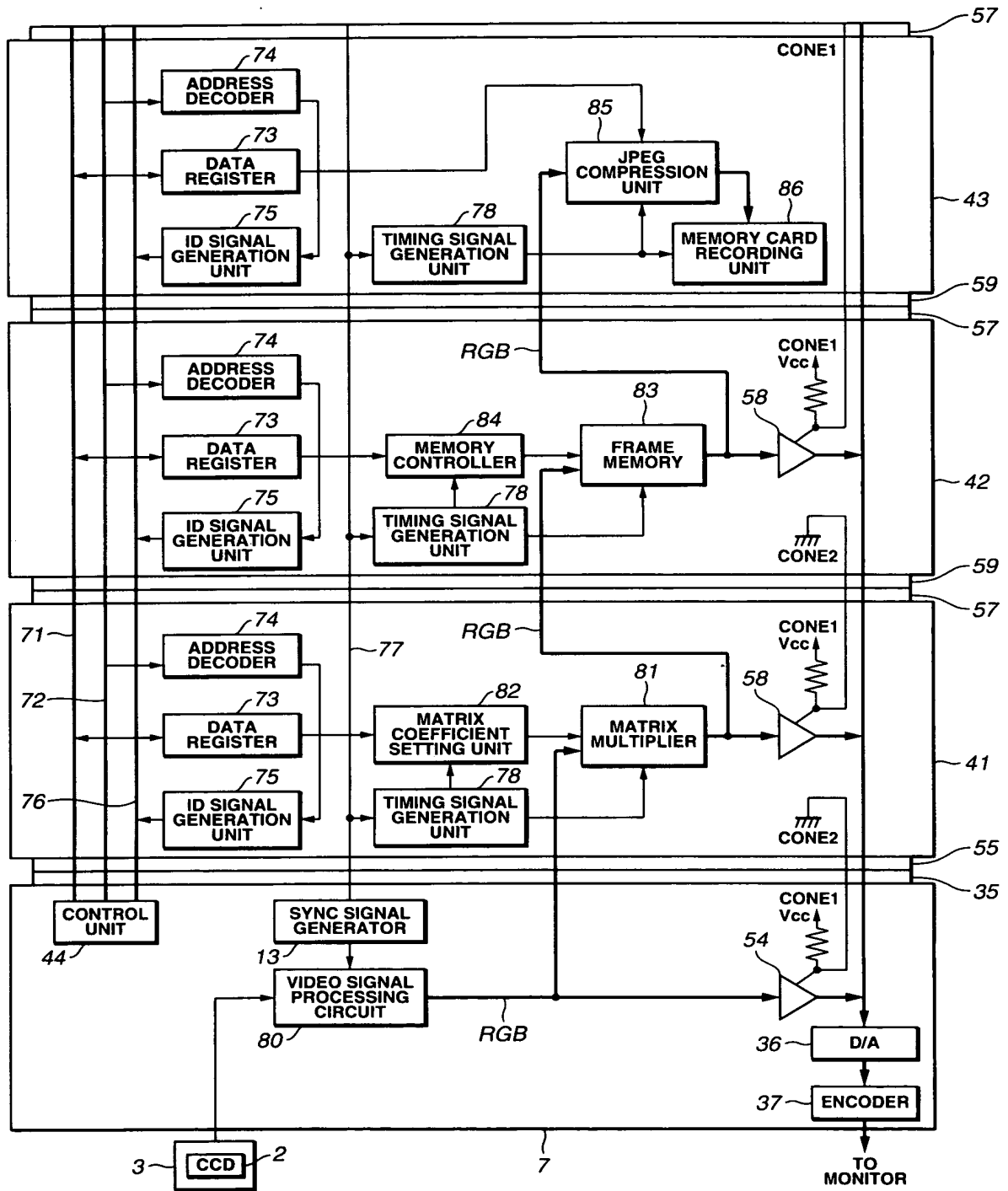
**FIG.5**



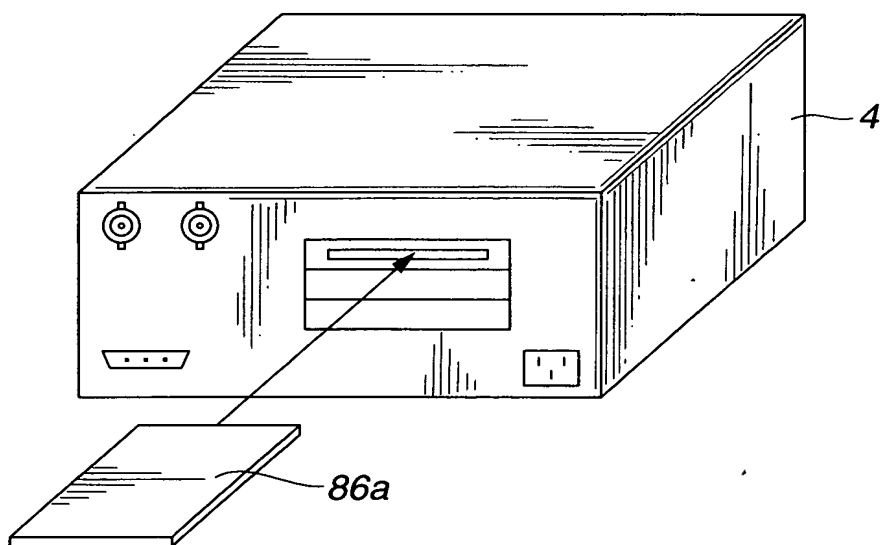
**FIG.7**



# FIG.6



**FIG.8**



# FIG.9

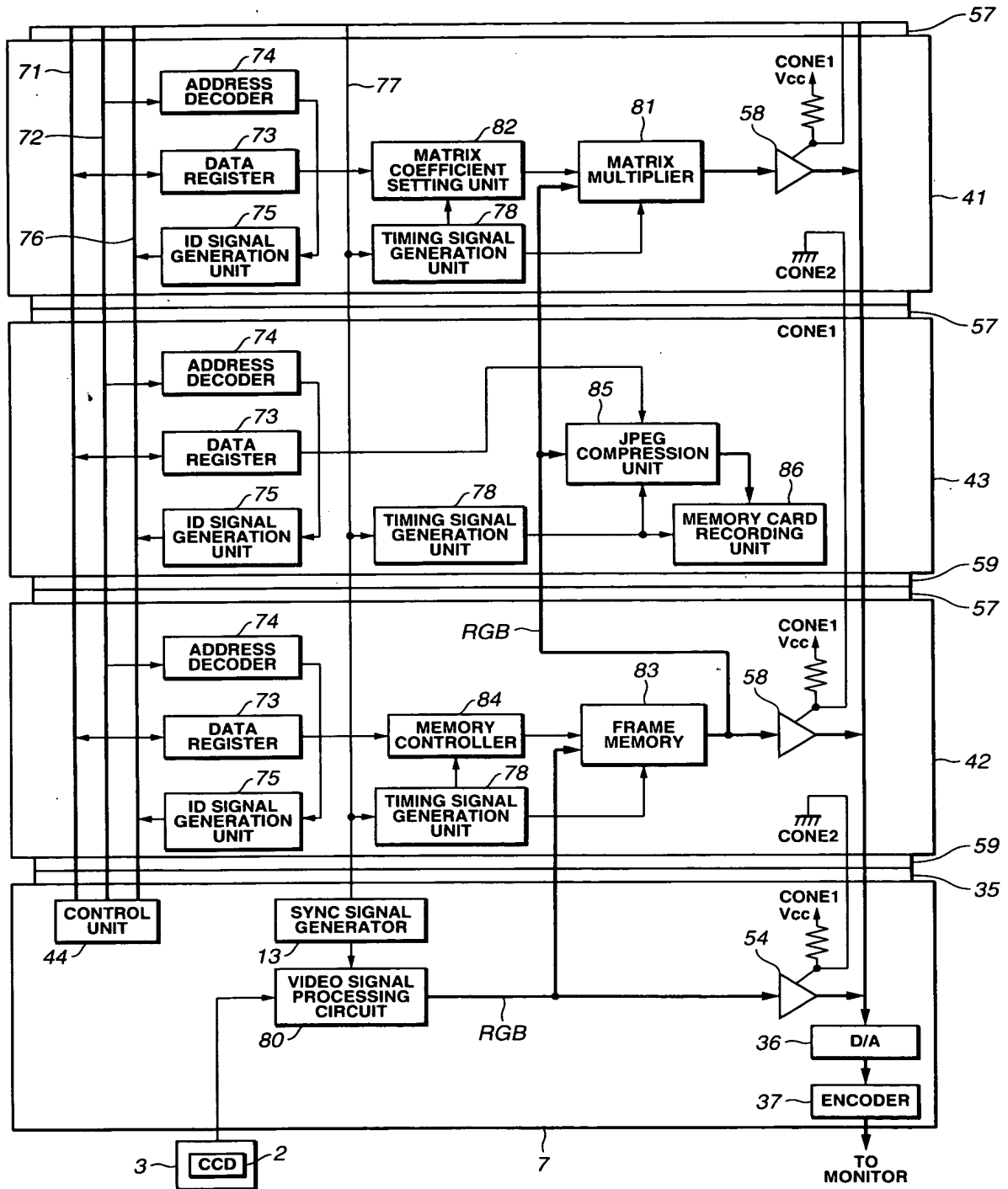
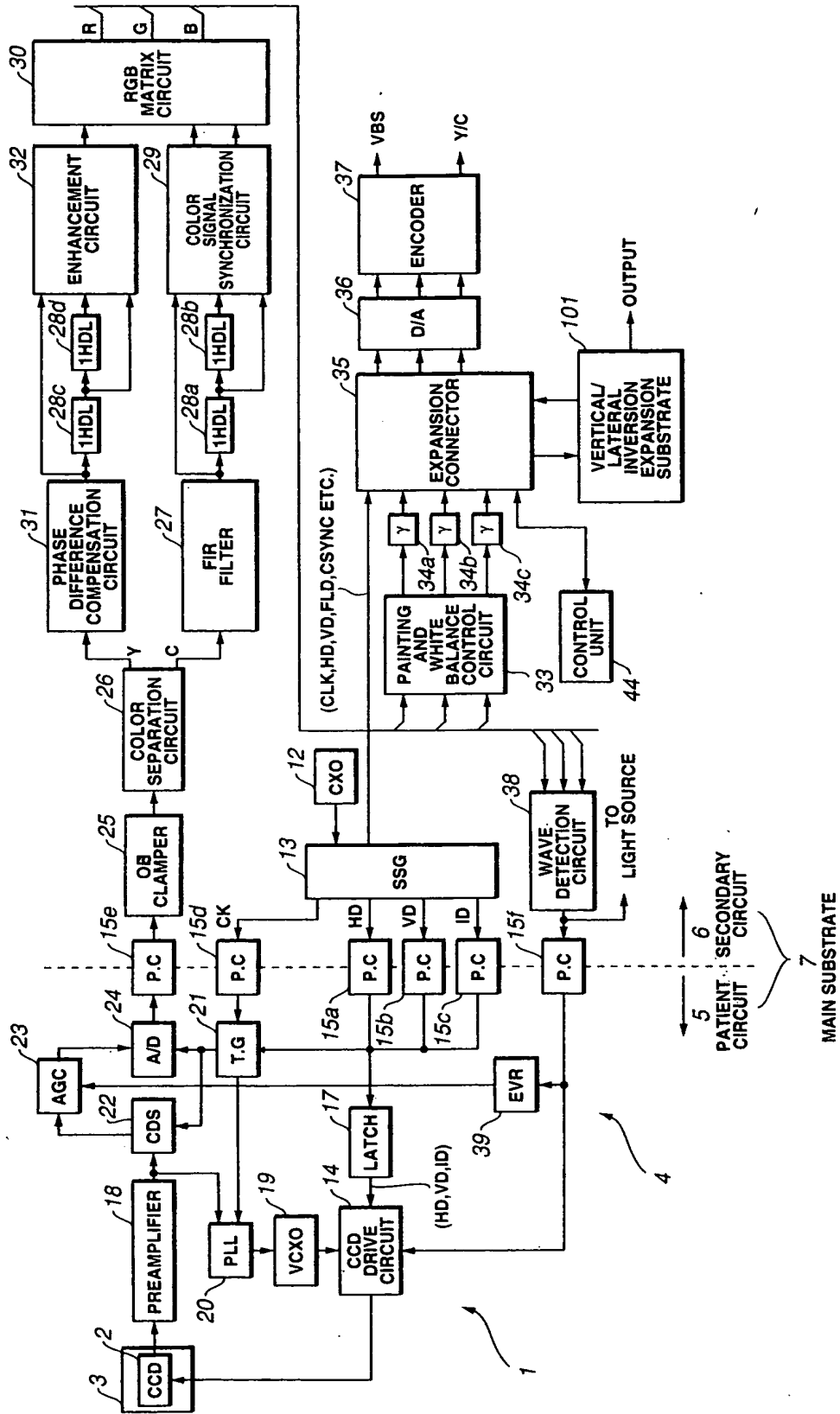
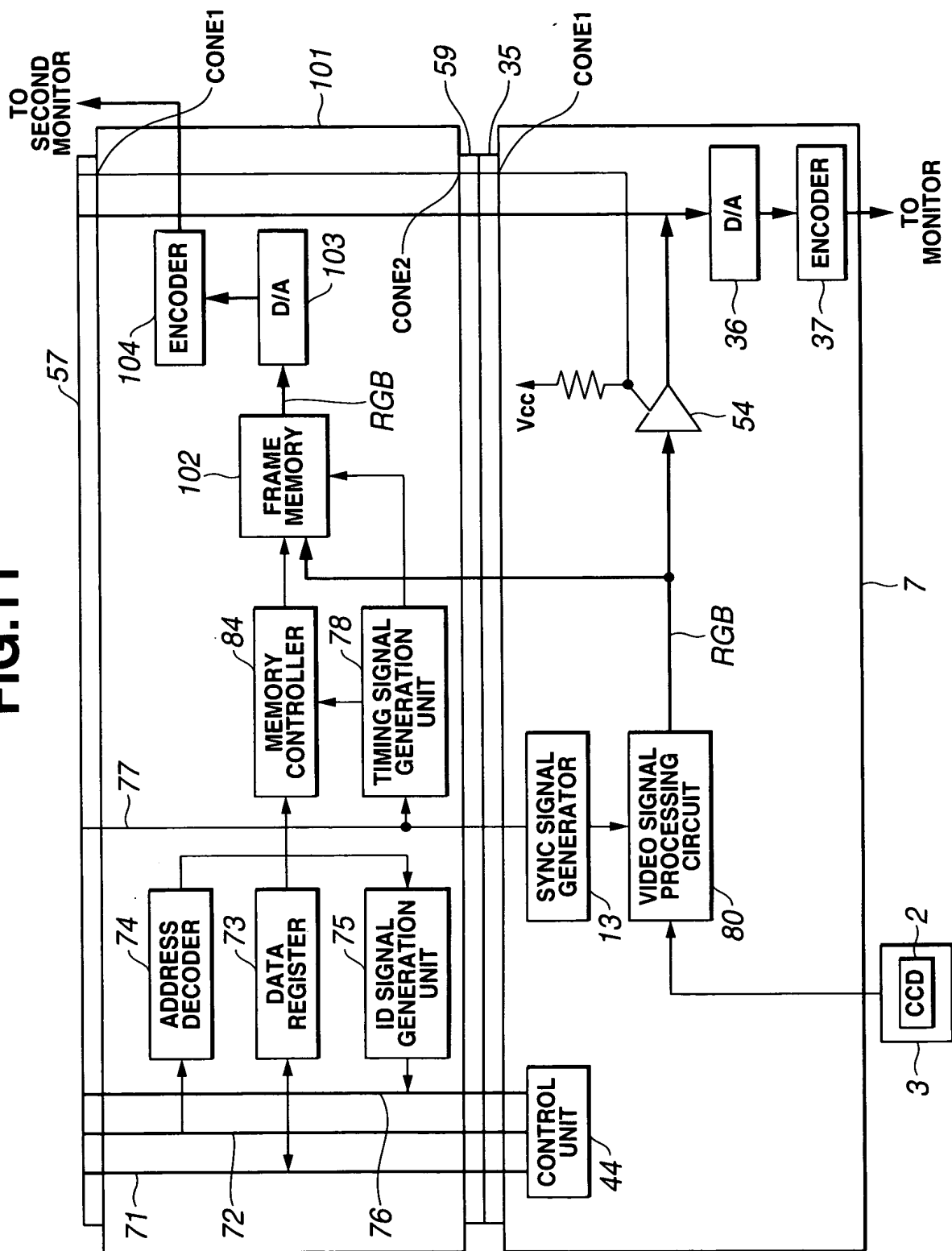




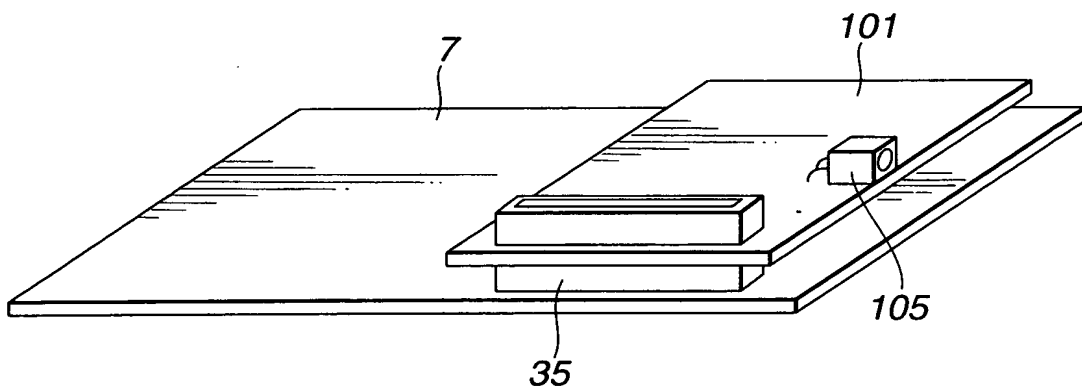
FIG. 10



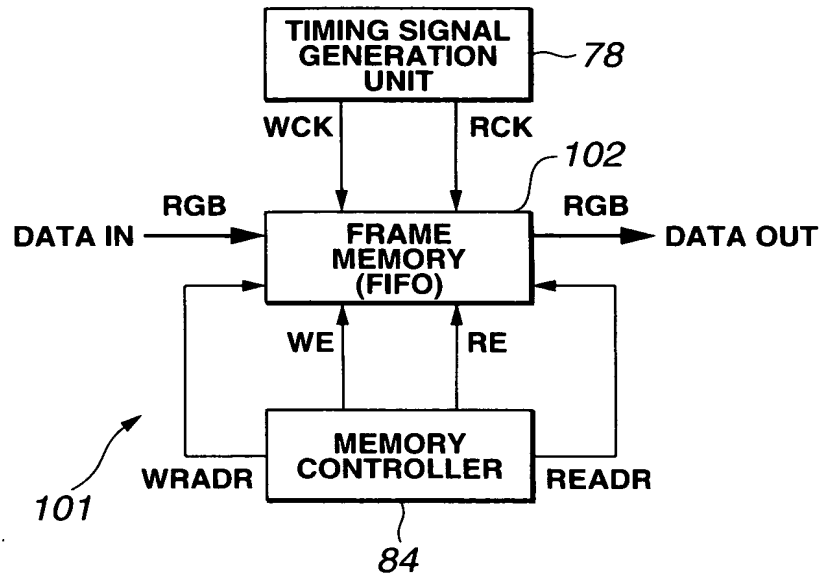
**FIG. 11**



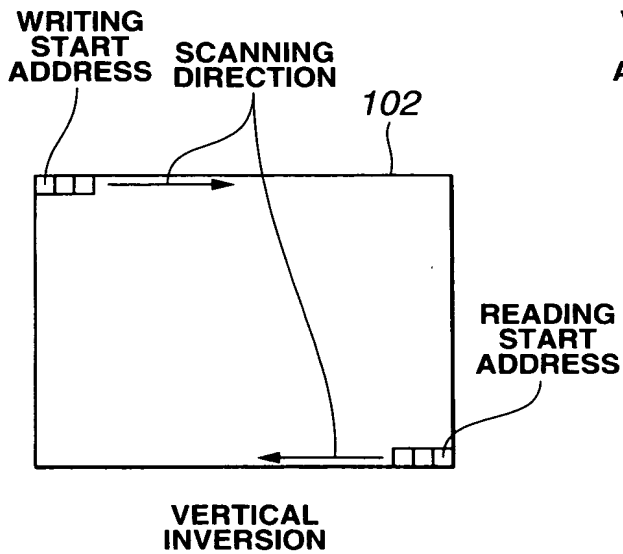
**FIG.12**



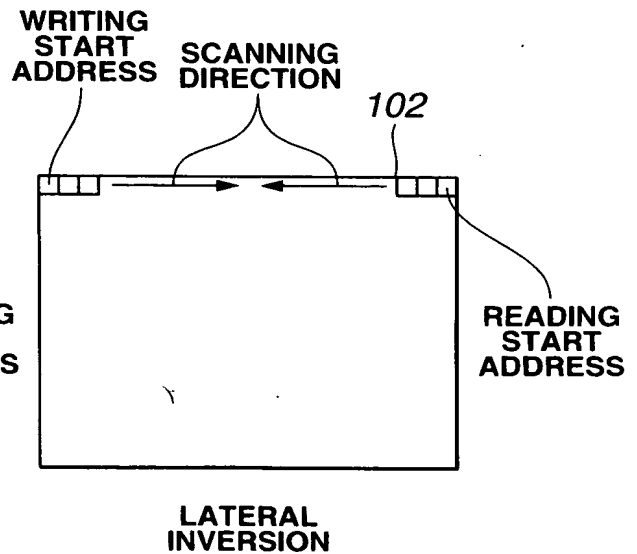
**FIG.13**



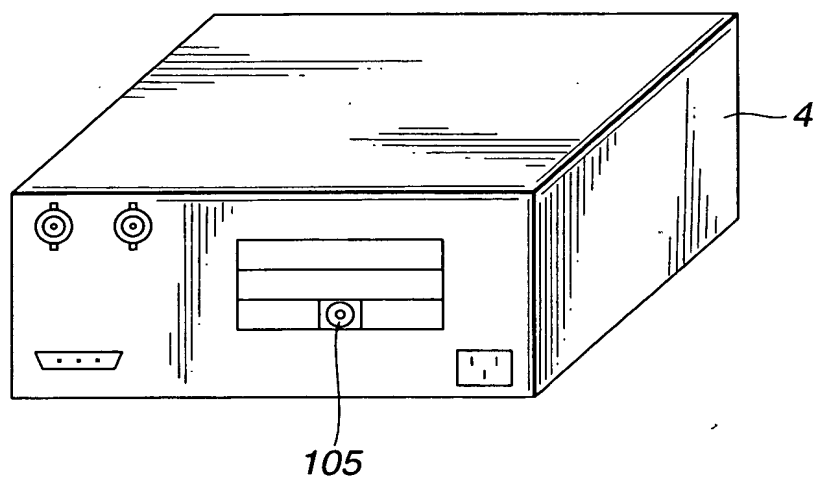
**FIG.14A**



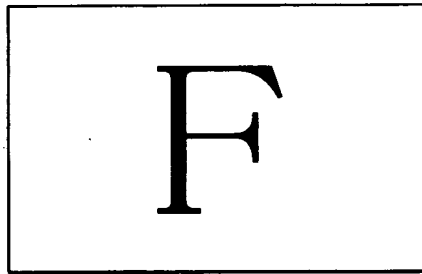
**FIG.14B**



**FIG.15**

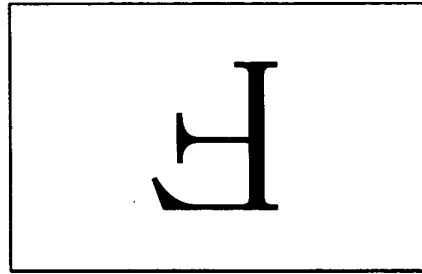


**FIG.16A**



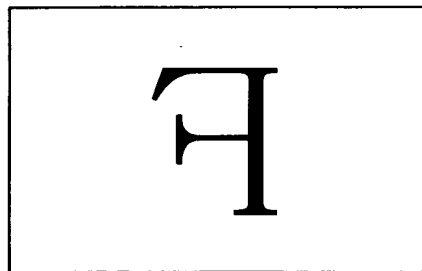
**NORMAL**

**FIG.16B**



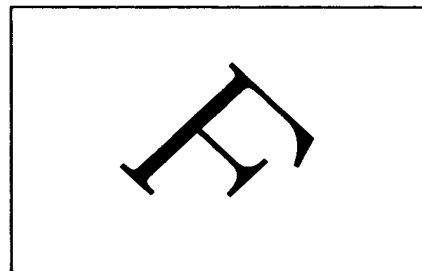
**VERTICAL  
INVERSION**

**FIG.16C**



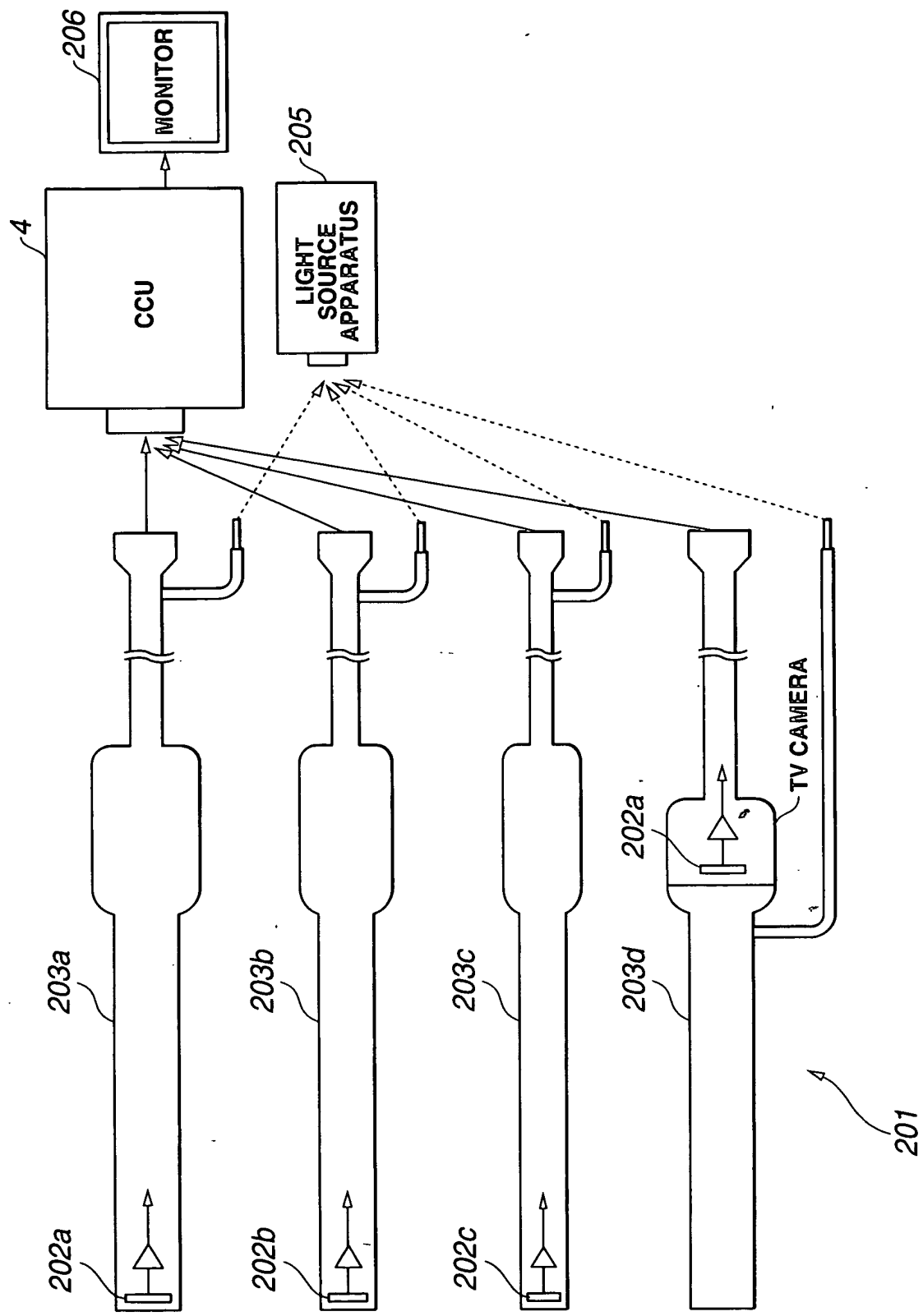
**LATERAL  
INVERSION**

**FIG.16D**

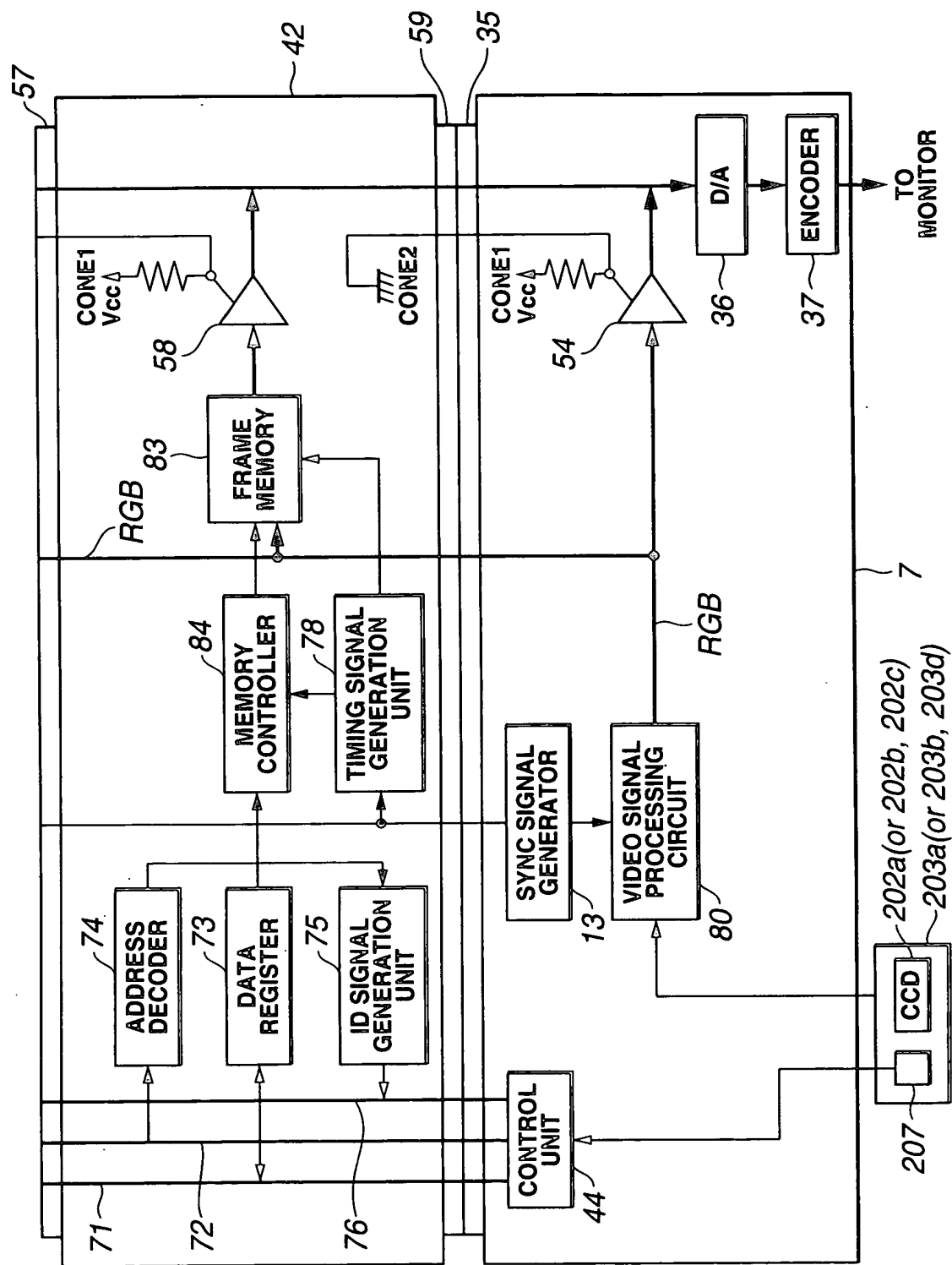


**ROTATION  
(EX. 45° RIGHT WARD)**

FIG. 17

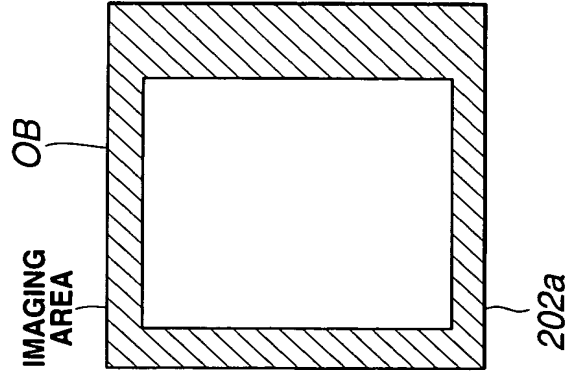


FILE

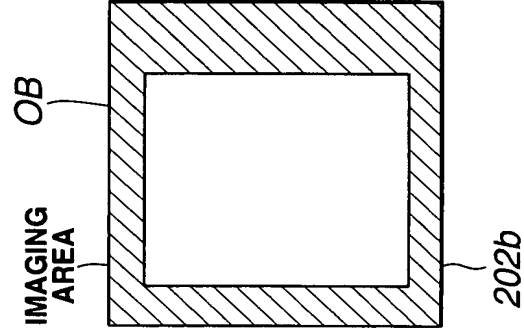




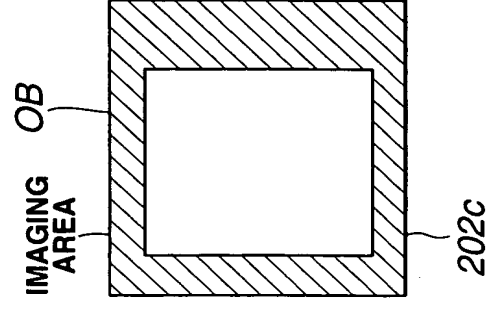
**FIG.19A**



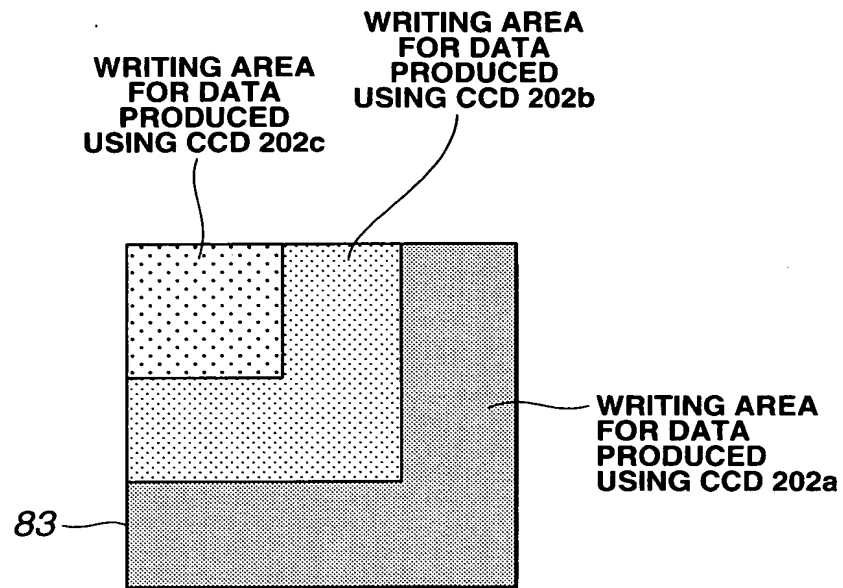
**FIG.19B**



**FIG.19C**



# FIG.20



# FIG.21

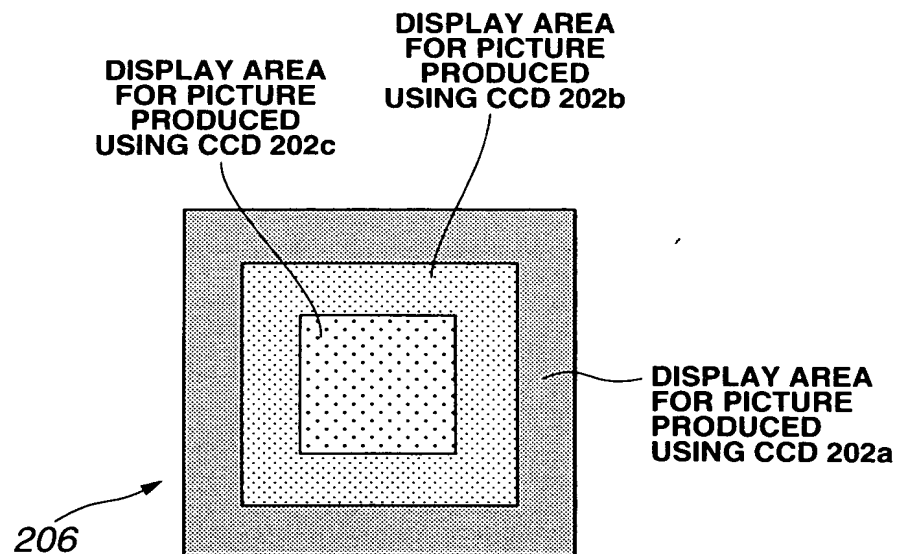


FIG.22

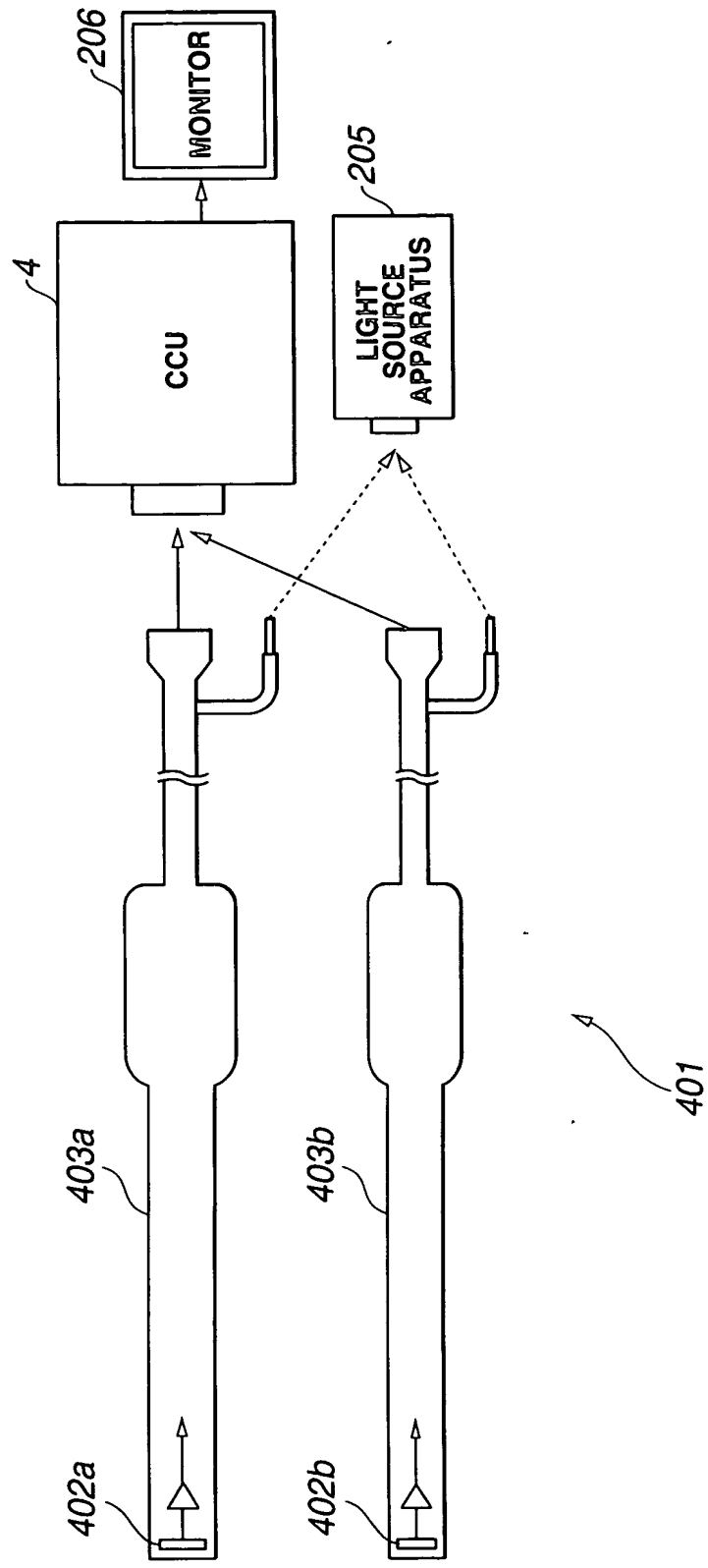


FIG.23

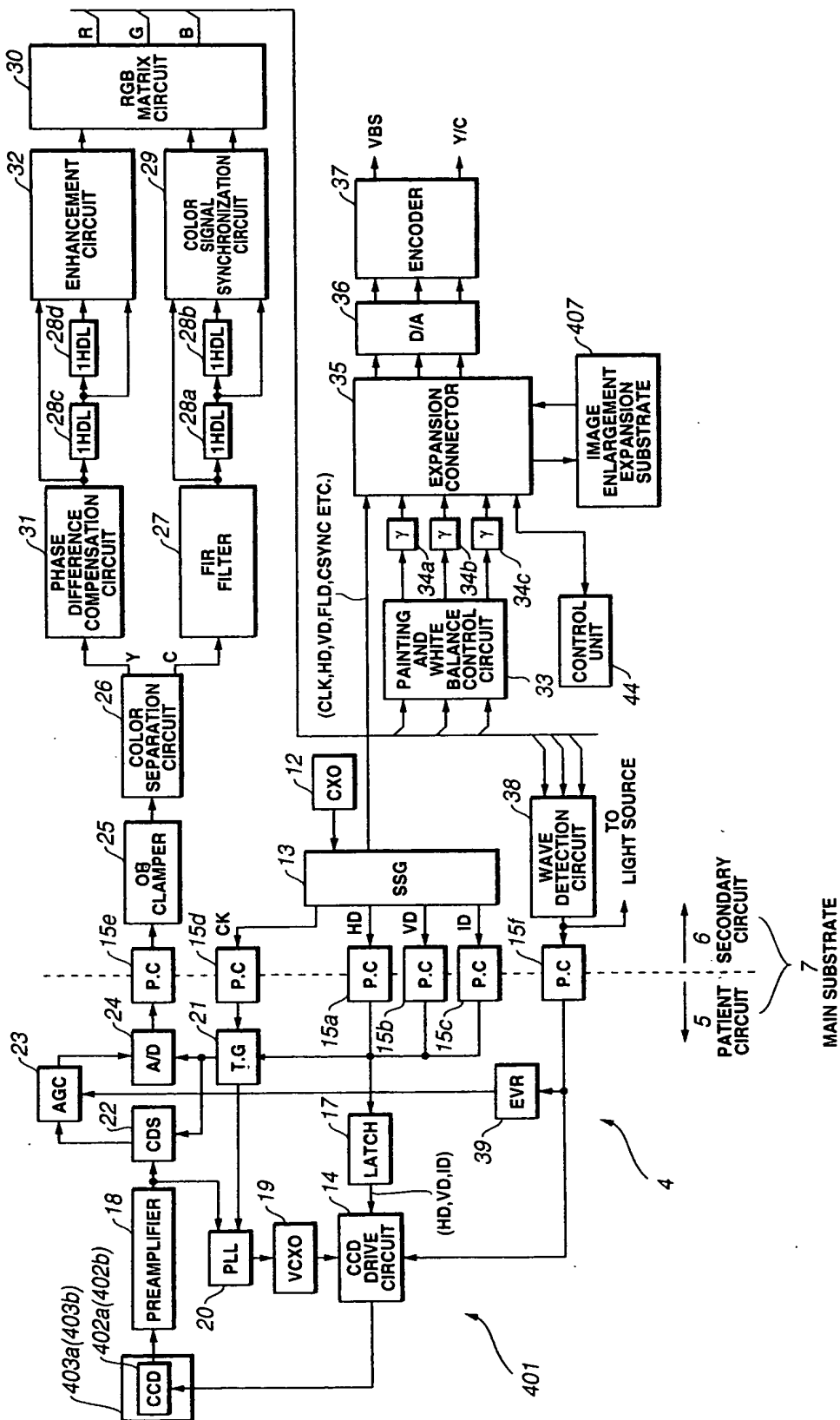


FIG. 24

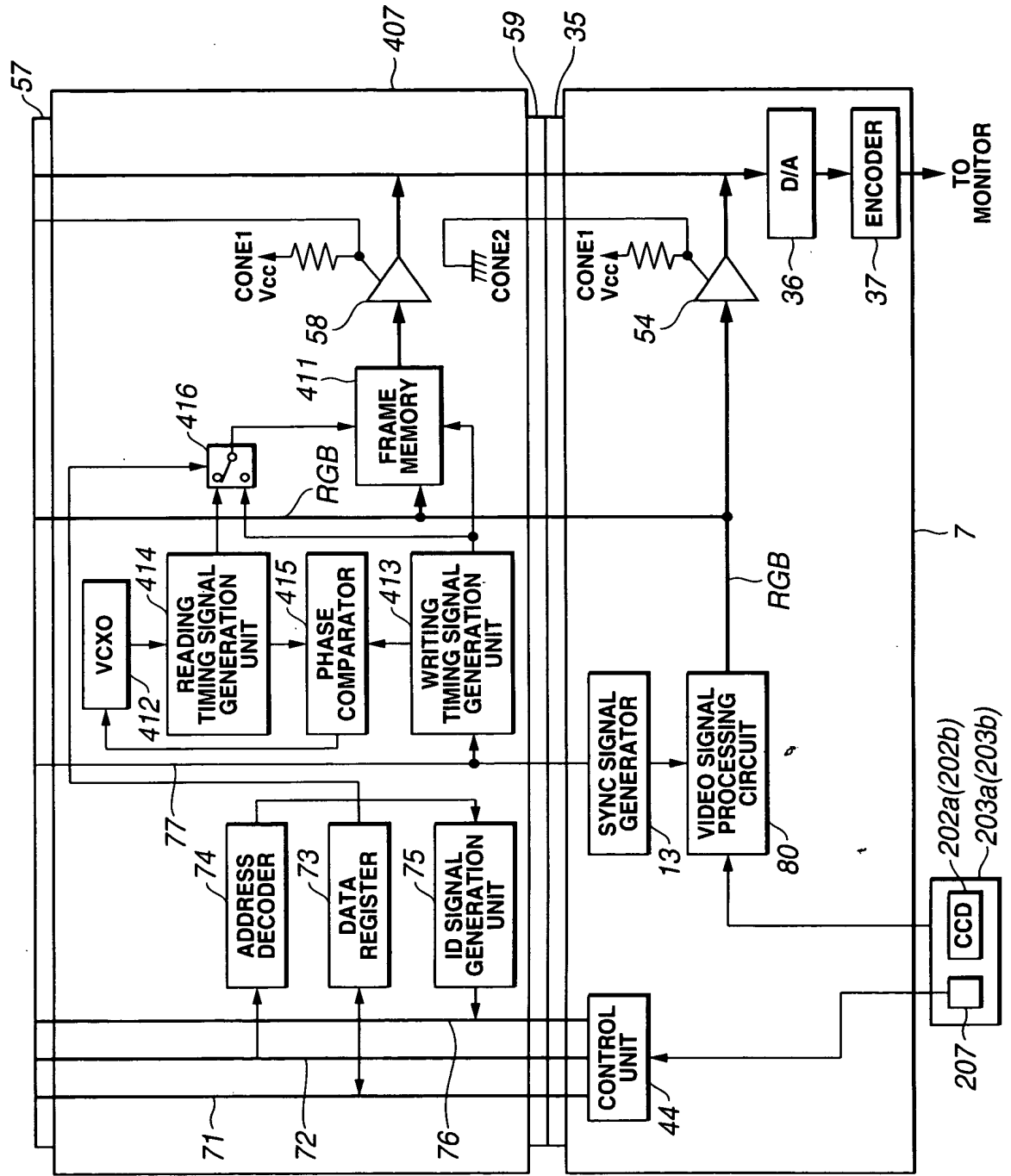


FIG.25

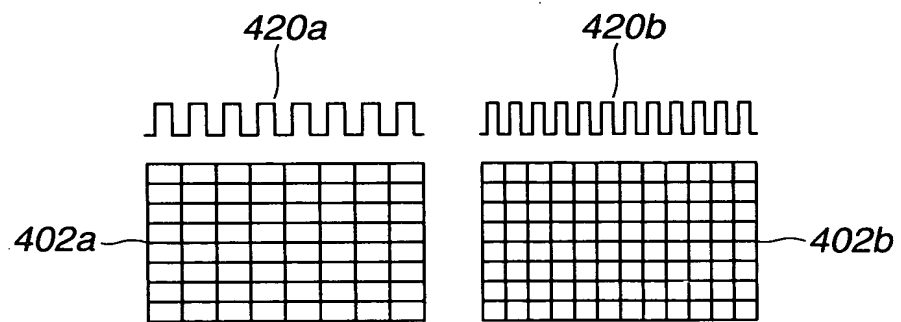


FIG.26

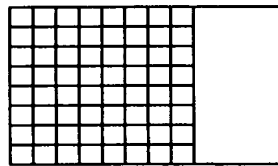


FIG.27A

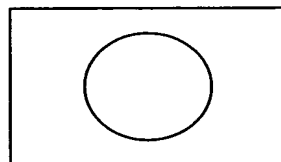


FIG.27B

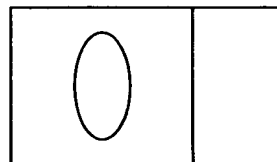


FIG. 28

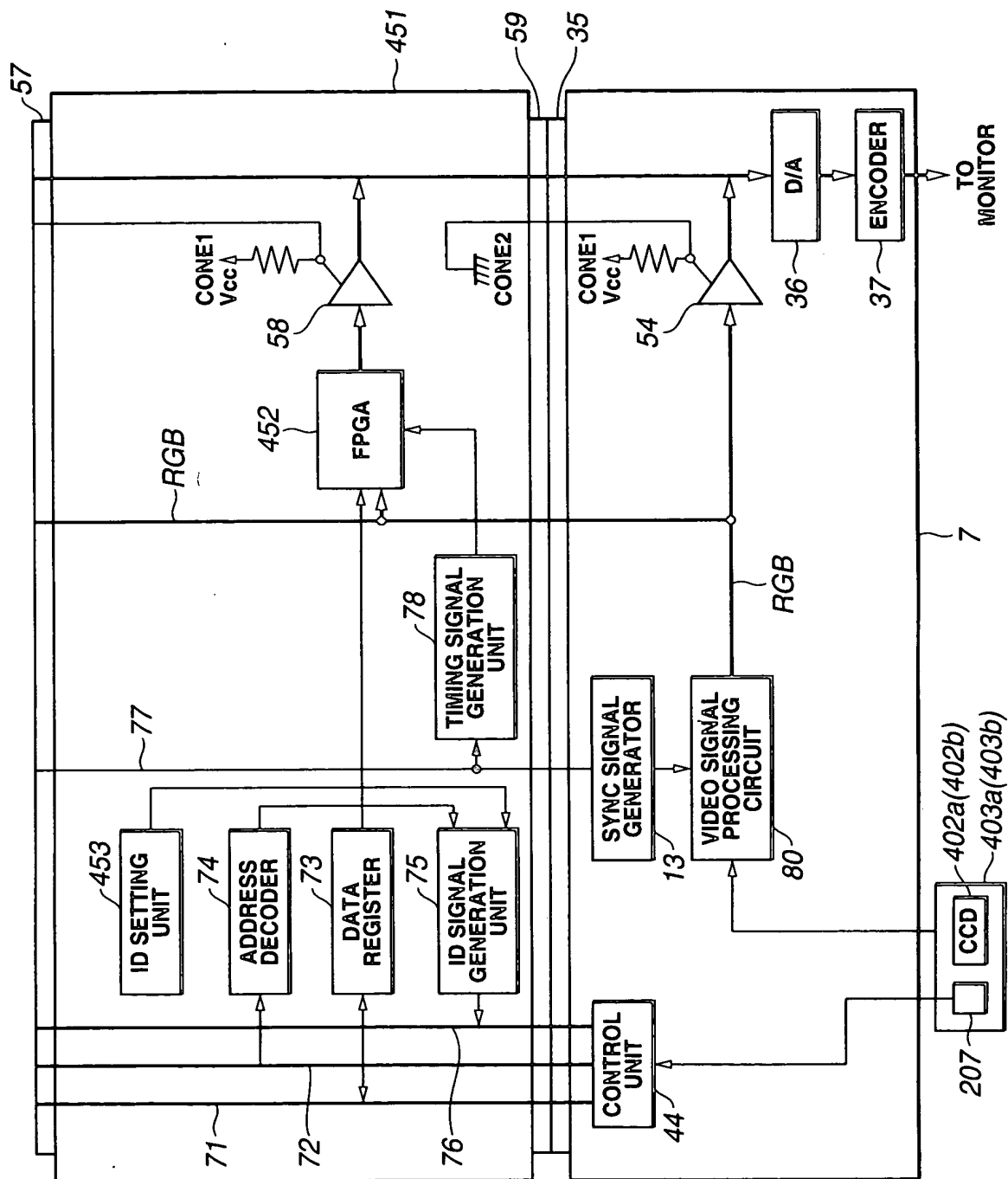


FIG.29

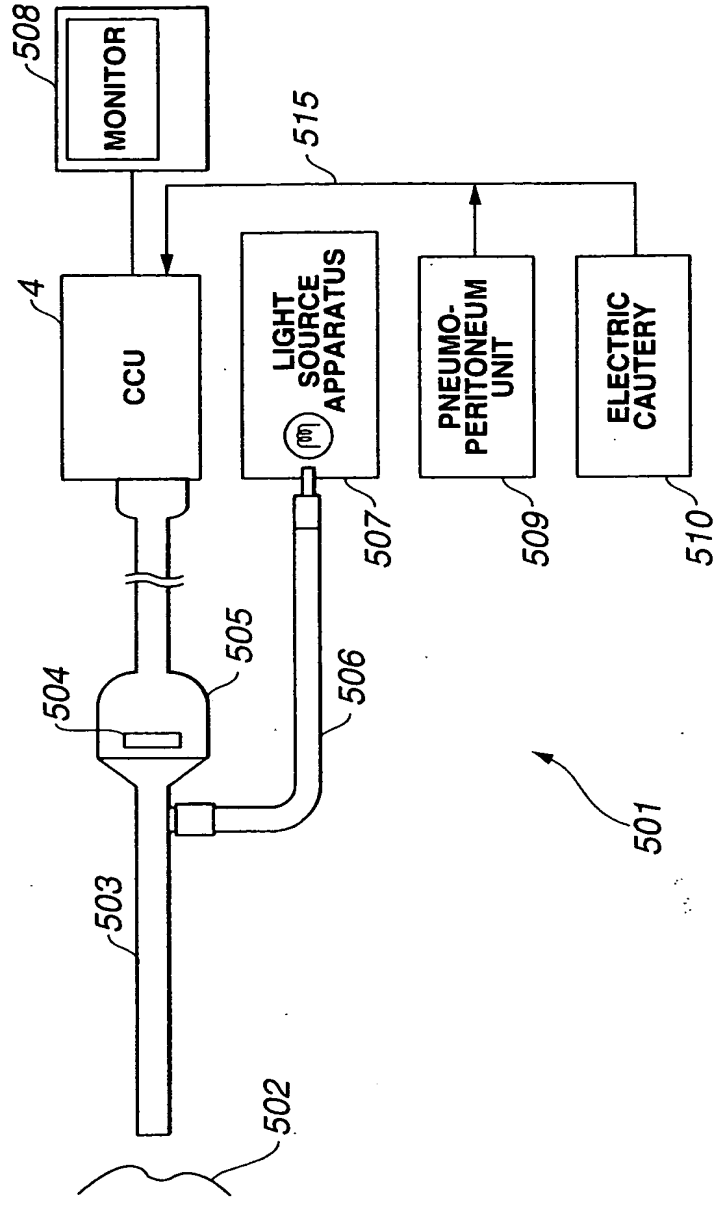




FIG.30

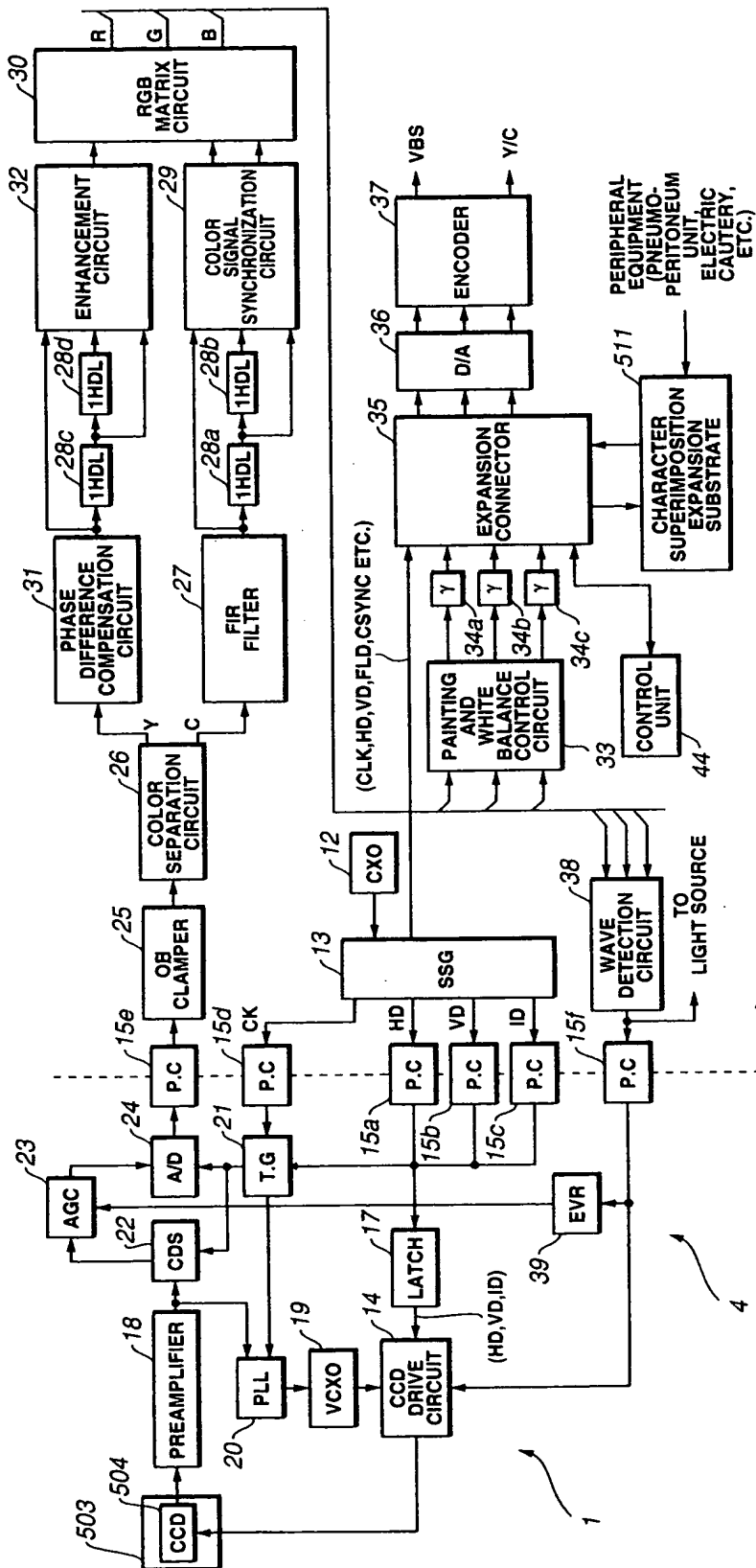
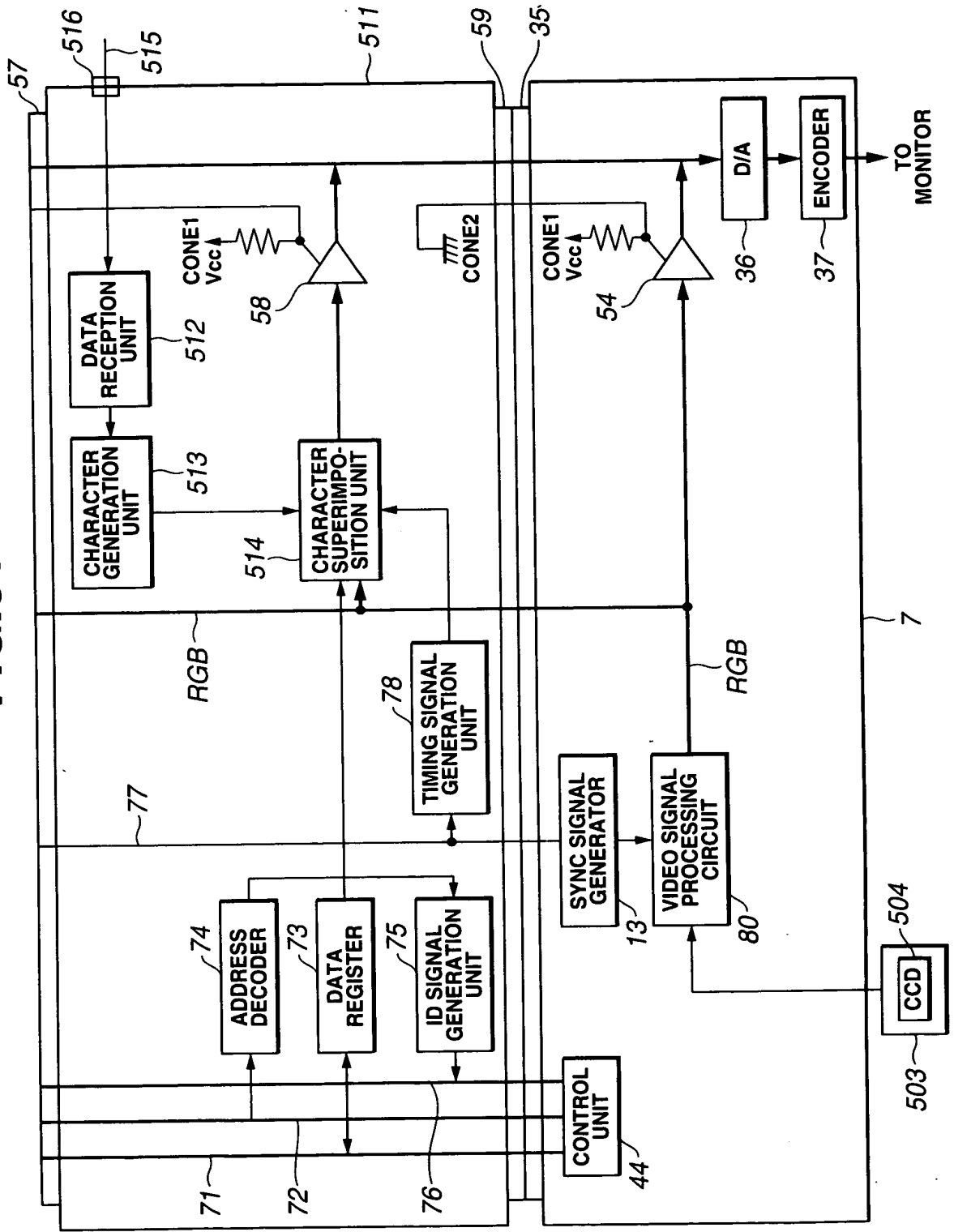


FIG.31



**FIG.32**

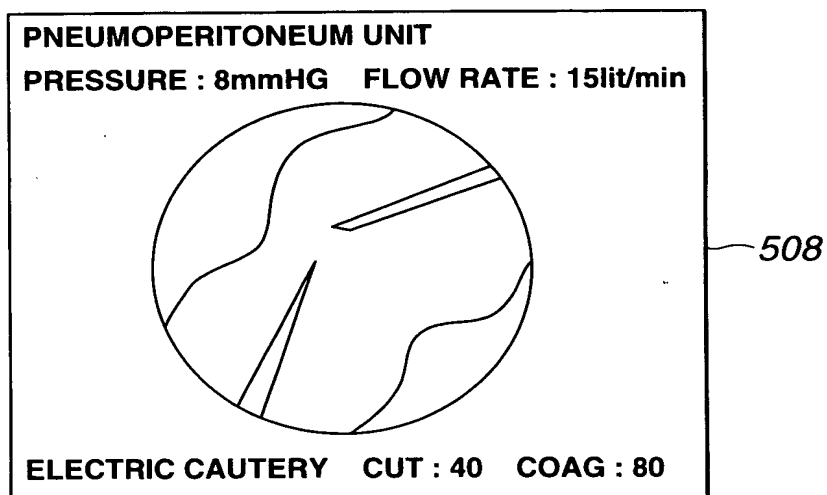


FIG. 33

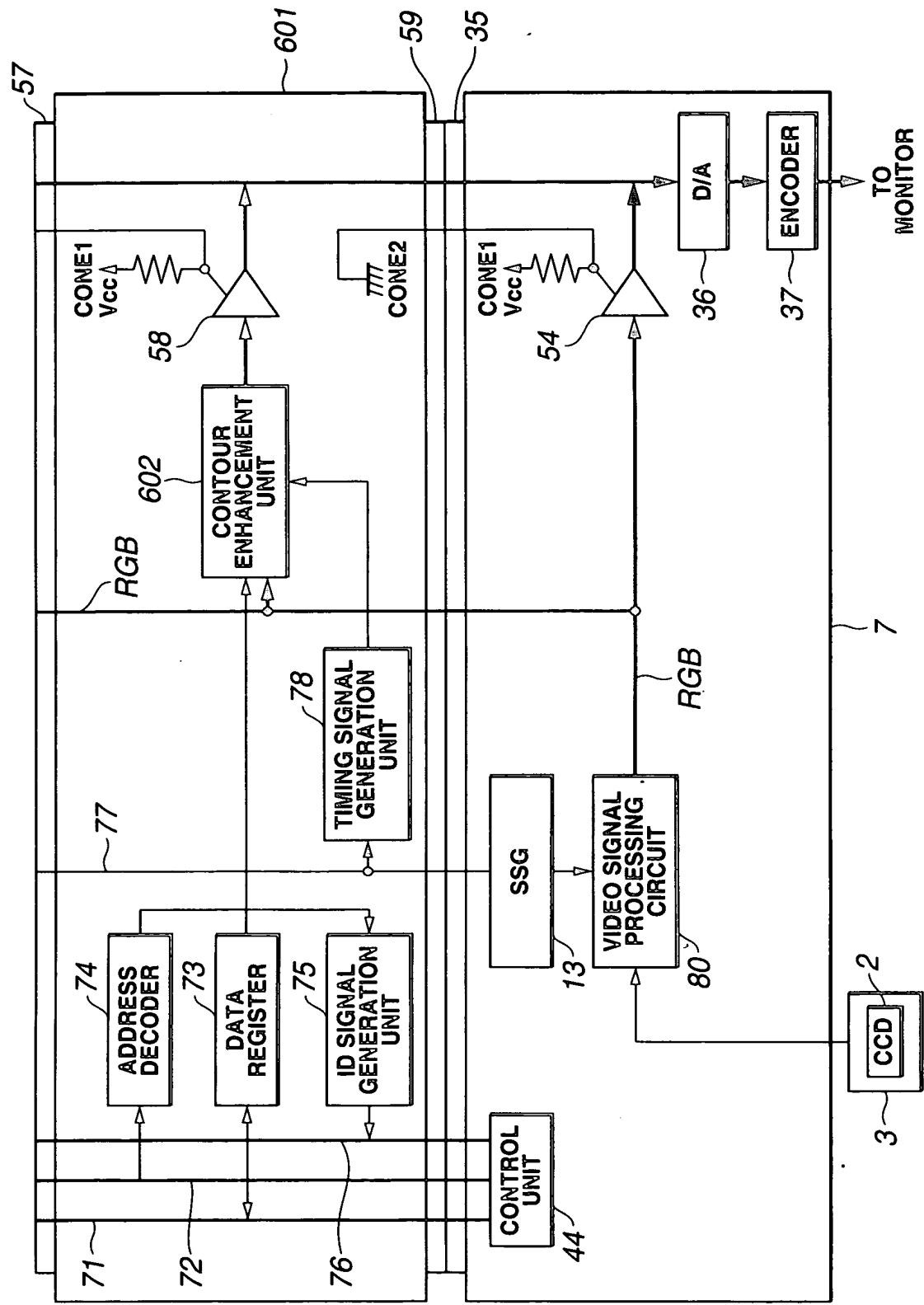
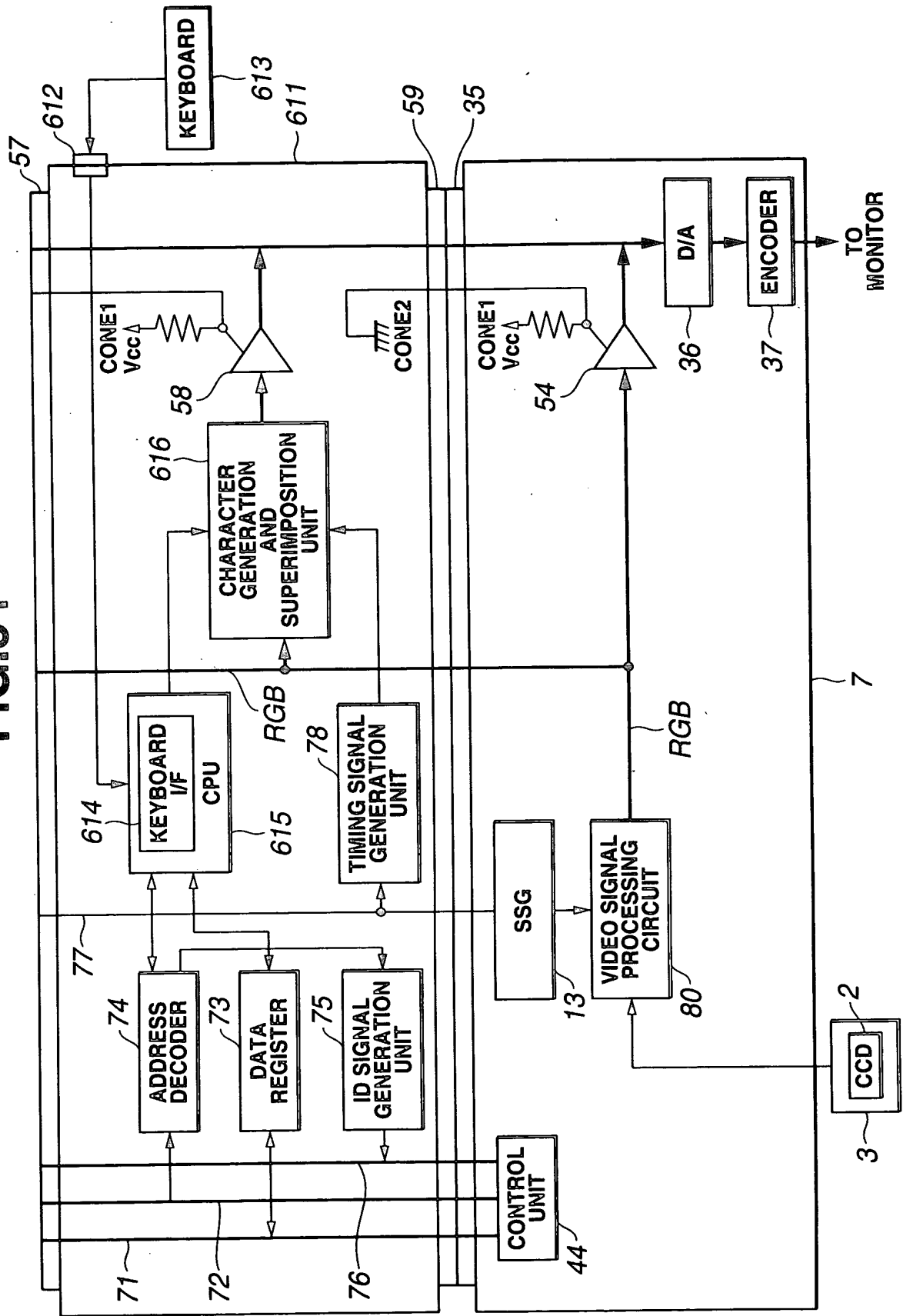


FIG. 34



The diagram illustrates a video camera system (7) with the following components and connections:

- Input Section (Left):** A **MICROPHONE** (623) is connected to a **VOICE RECOGNITION IC** (616) via a **CONNECTION 1** (622). The IC is also connected to a **CPU** (625) via a **CONNECTION 2** (624). The CPU is connected to an **ADDRESS DECODER** (74) and a **DATA REGISTER** (73).
- Control Section (Bottom):** A **CONTROL UNIT** (44) is connected to the **ADDRESS DECODER** (74), **DATA REGISTER** (73), and an **ID SIGNAL GENERATION UNIT** (75). The ID unit is connected to a **TIMING SIGNAL GENERATION UNIT** (78).
- Processing Section (Middle):** The **CHARACTER GENERATION AND SUPERIMPOSITION UNIT** (616) receives input from the **VOICE RECOGNITION IC** (616) and the **TIMING SIGNAL GENERATION UNIT** (78). It outputs an **RGB** signal to the **VIDEO SIGNAL PROCESSING CIRCUIT** (80).
- Output Section (Right):** The **VIDEO SIGNAL PROCESSING CIRCUIT** (80) is connected to an **SSG** (13) and a **D/A** (36). The D/A is connected to an **ENCODER** (37), which outputs **TO MONITOR**.
- Other Components:** A **CCD** (2) is connected to the **VIDEO SIGNAL PROCESSING CIRCUIT** (80). A **CONNECTION 1** (54) and **CONNECTION 2** (58) are also shown, likely for external connections.

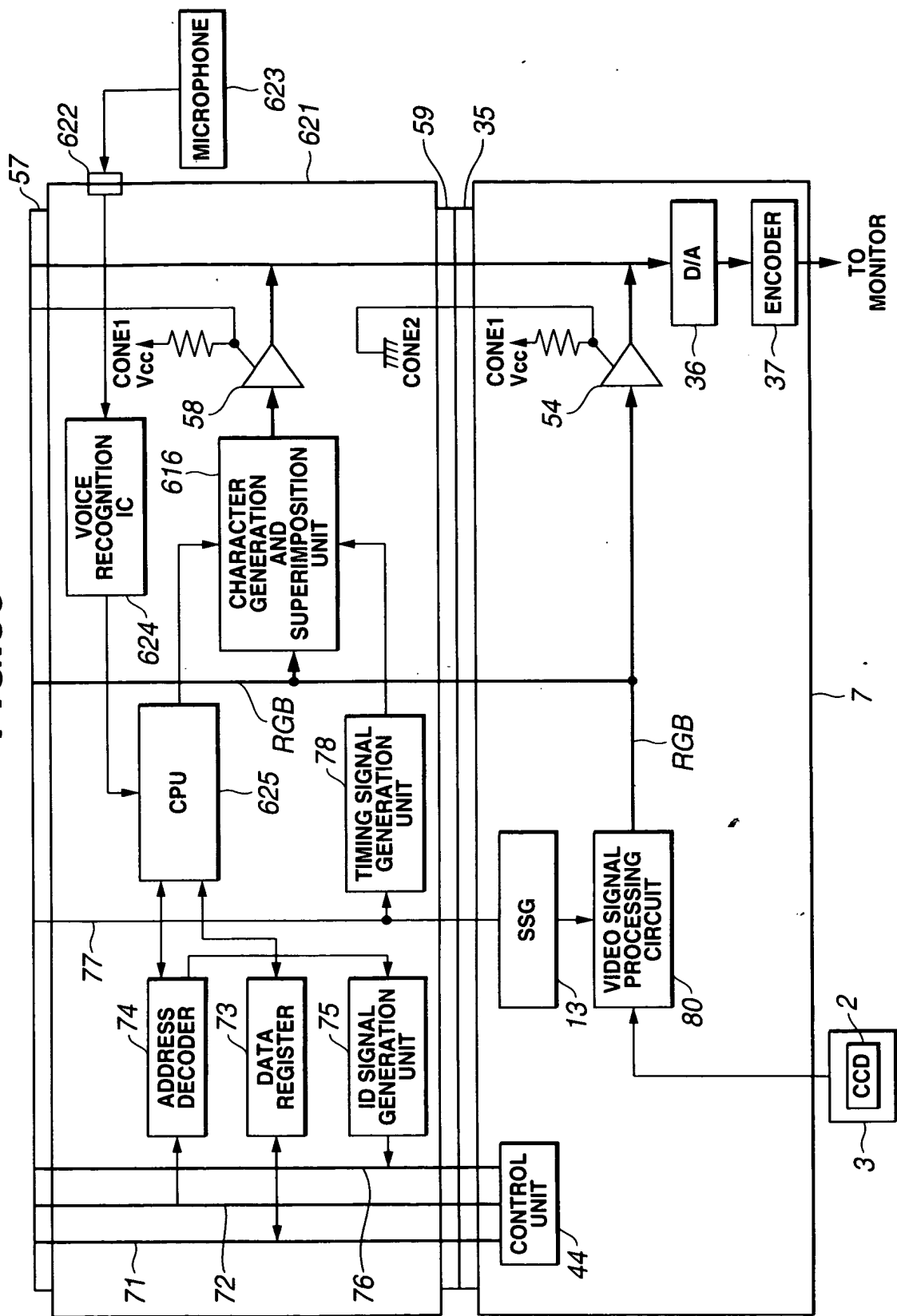


FIG.36

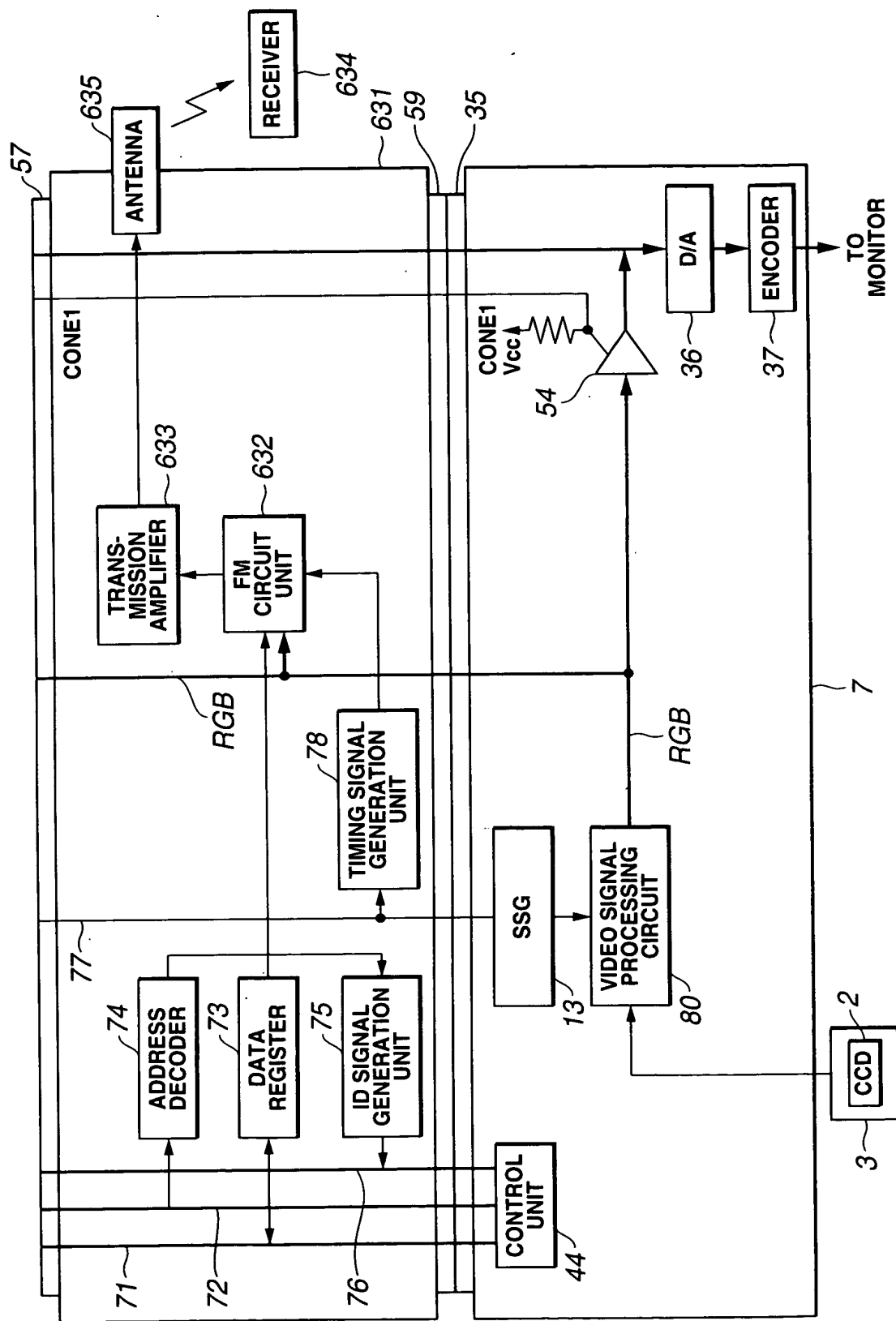


FIG.37

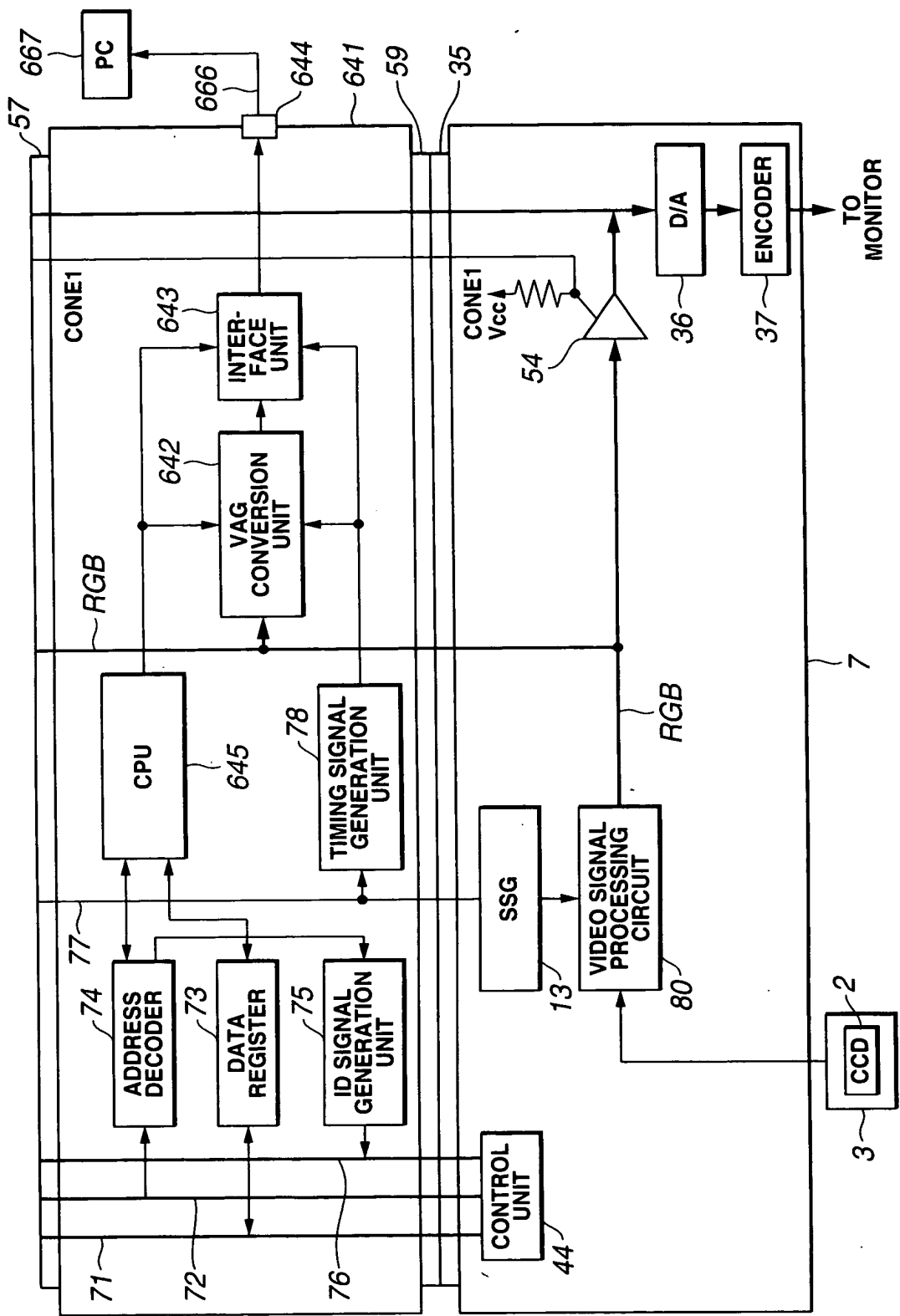




FIG.38

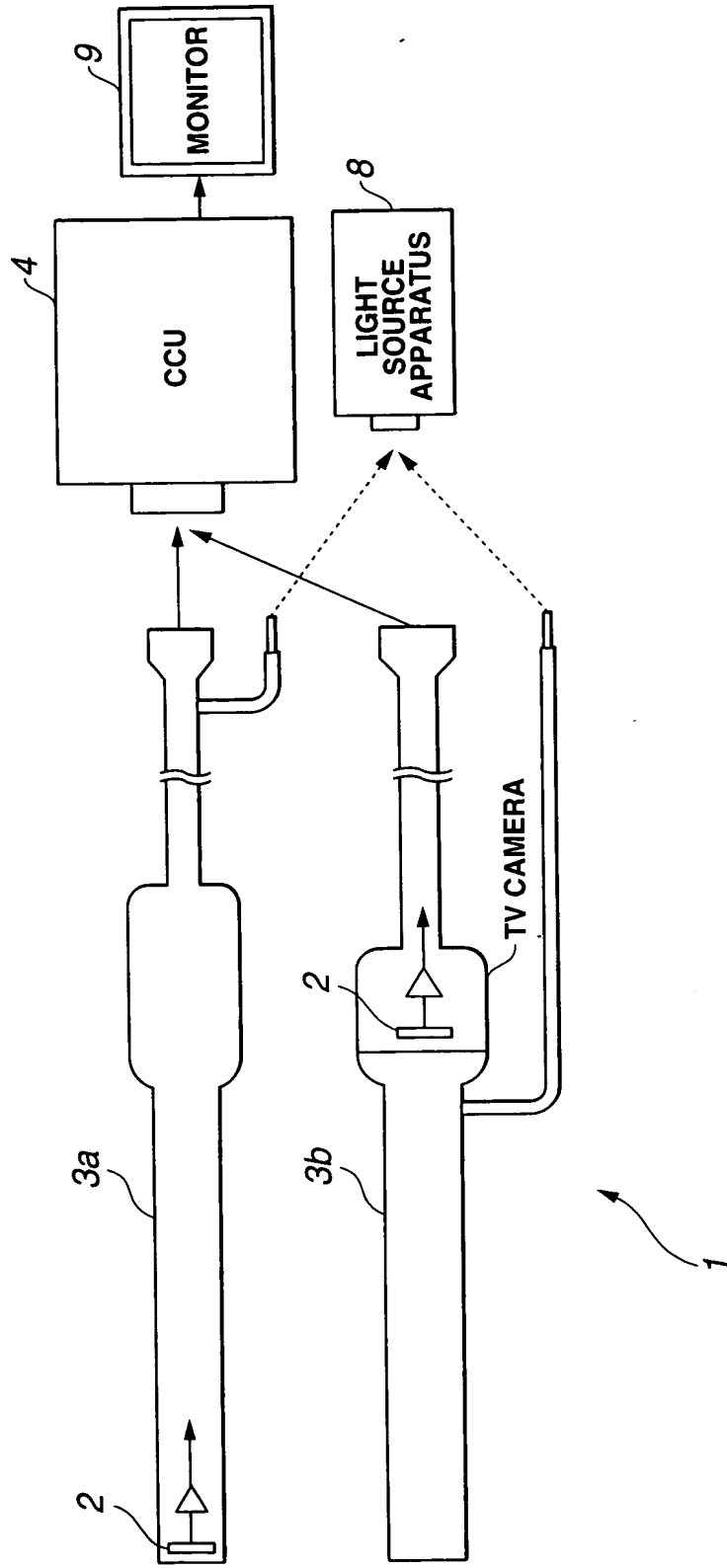
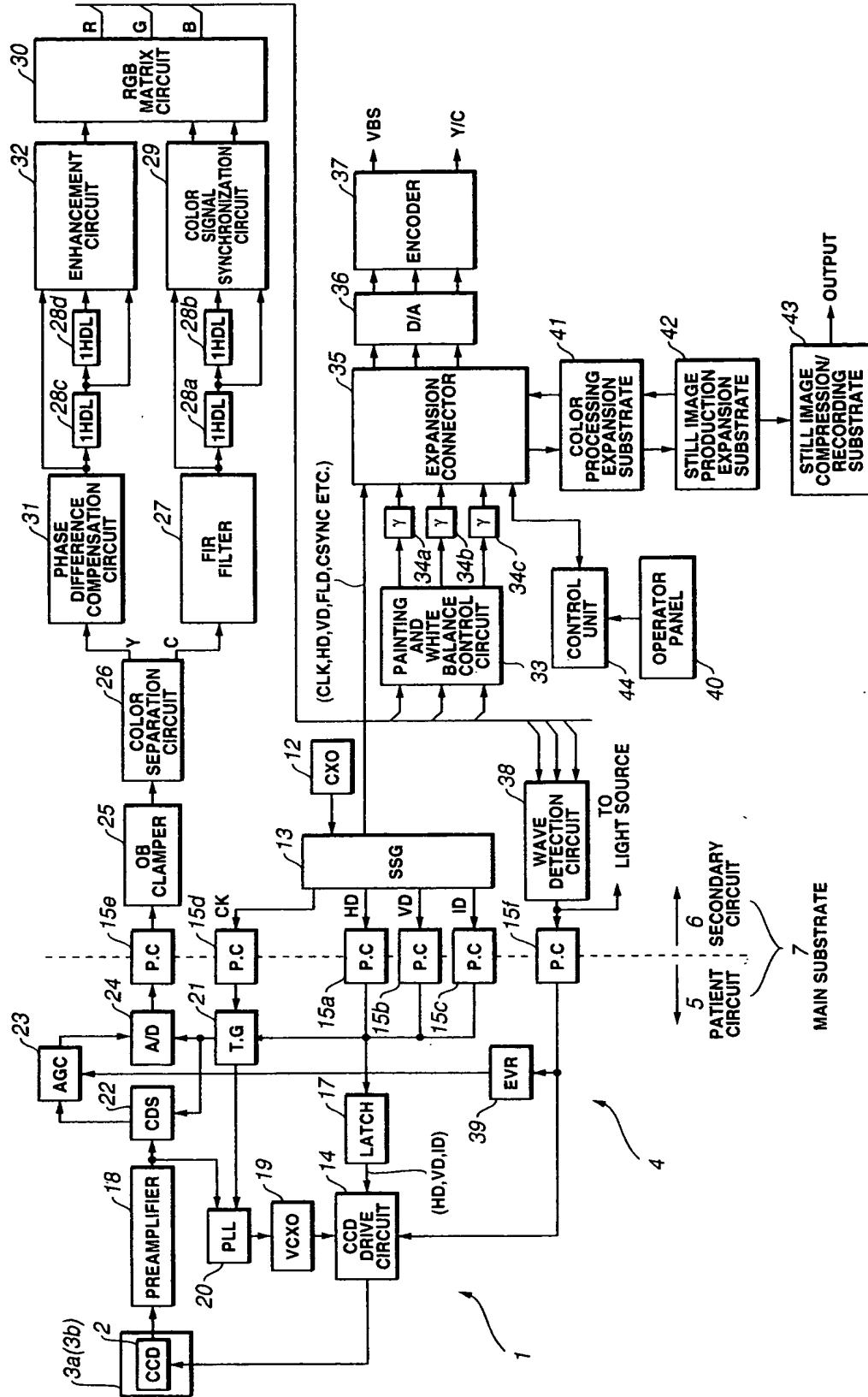
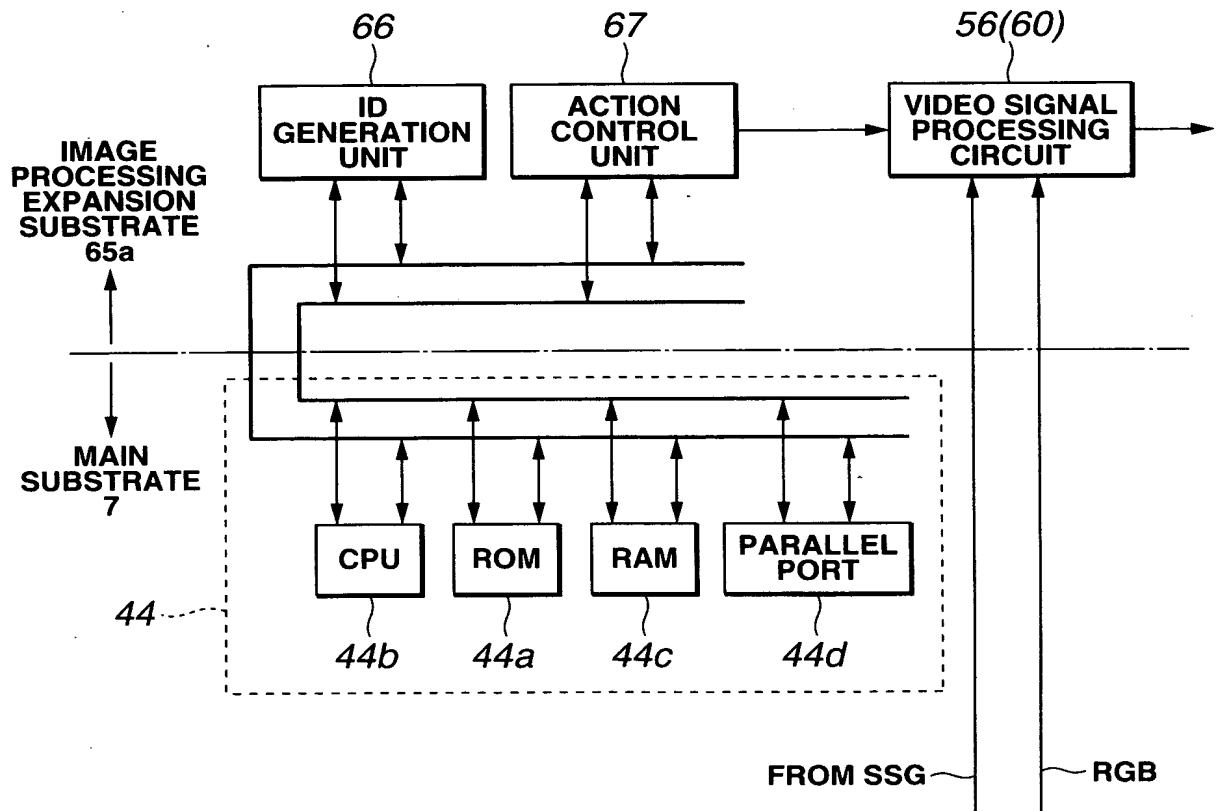


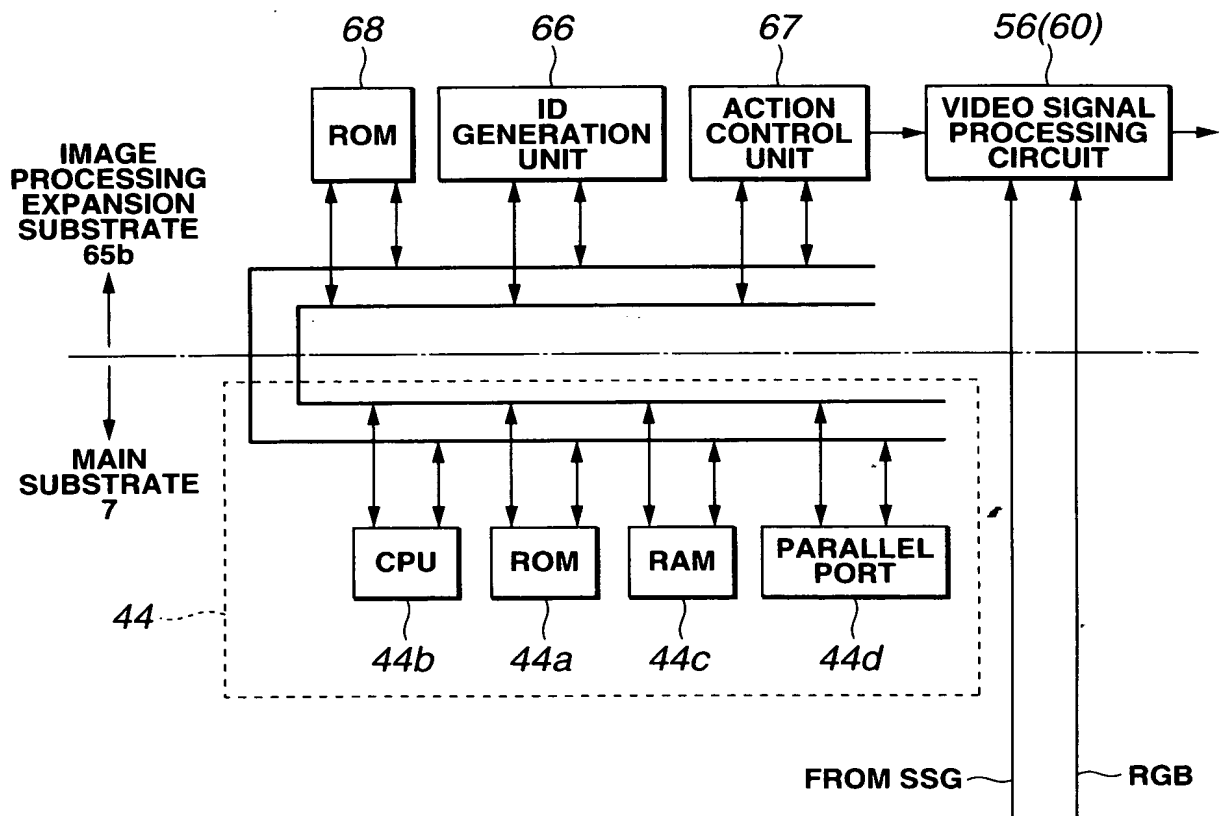
FIG.39



**FIG.40**



**FIG.41**



# FIG.42

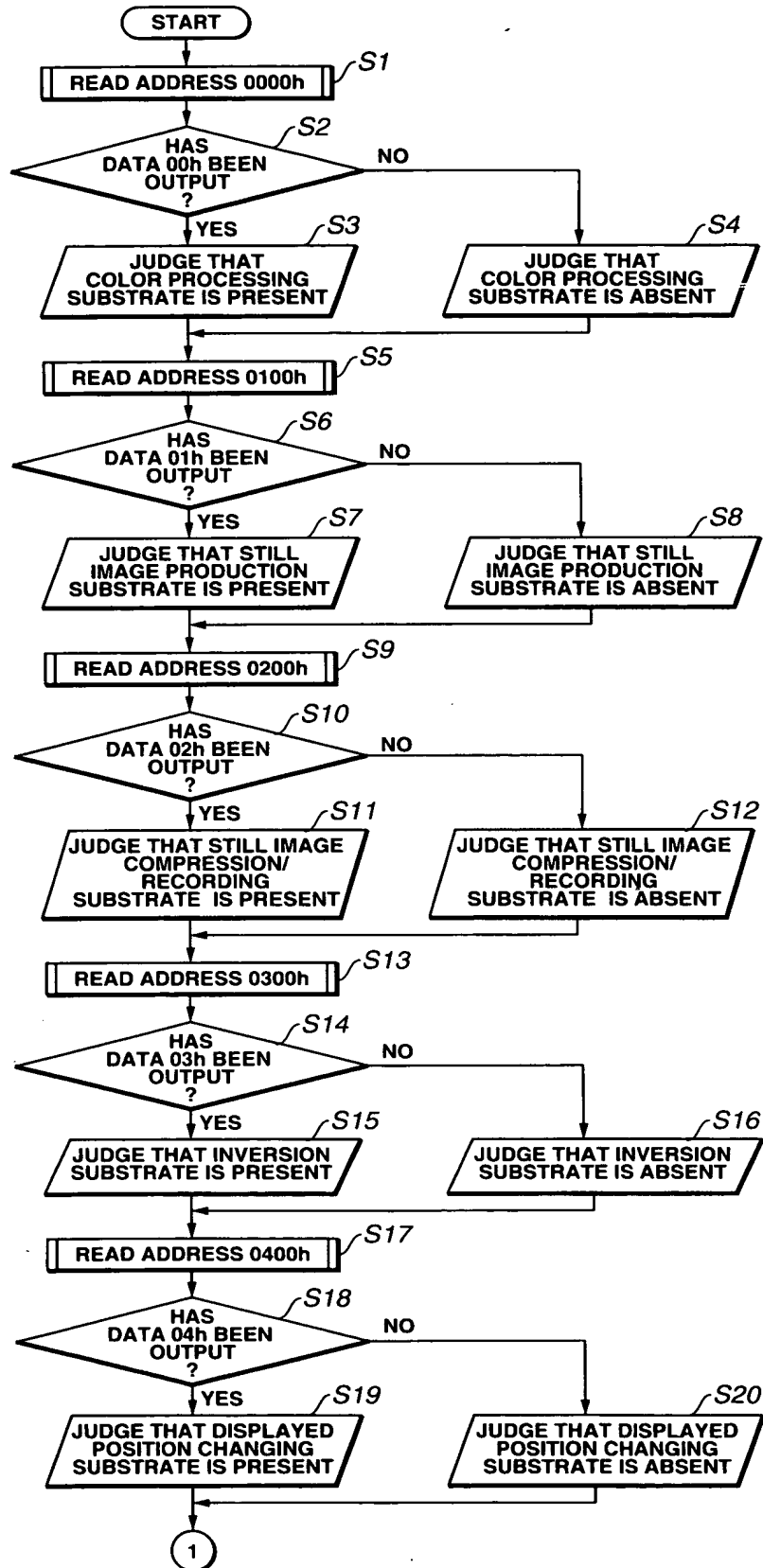
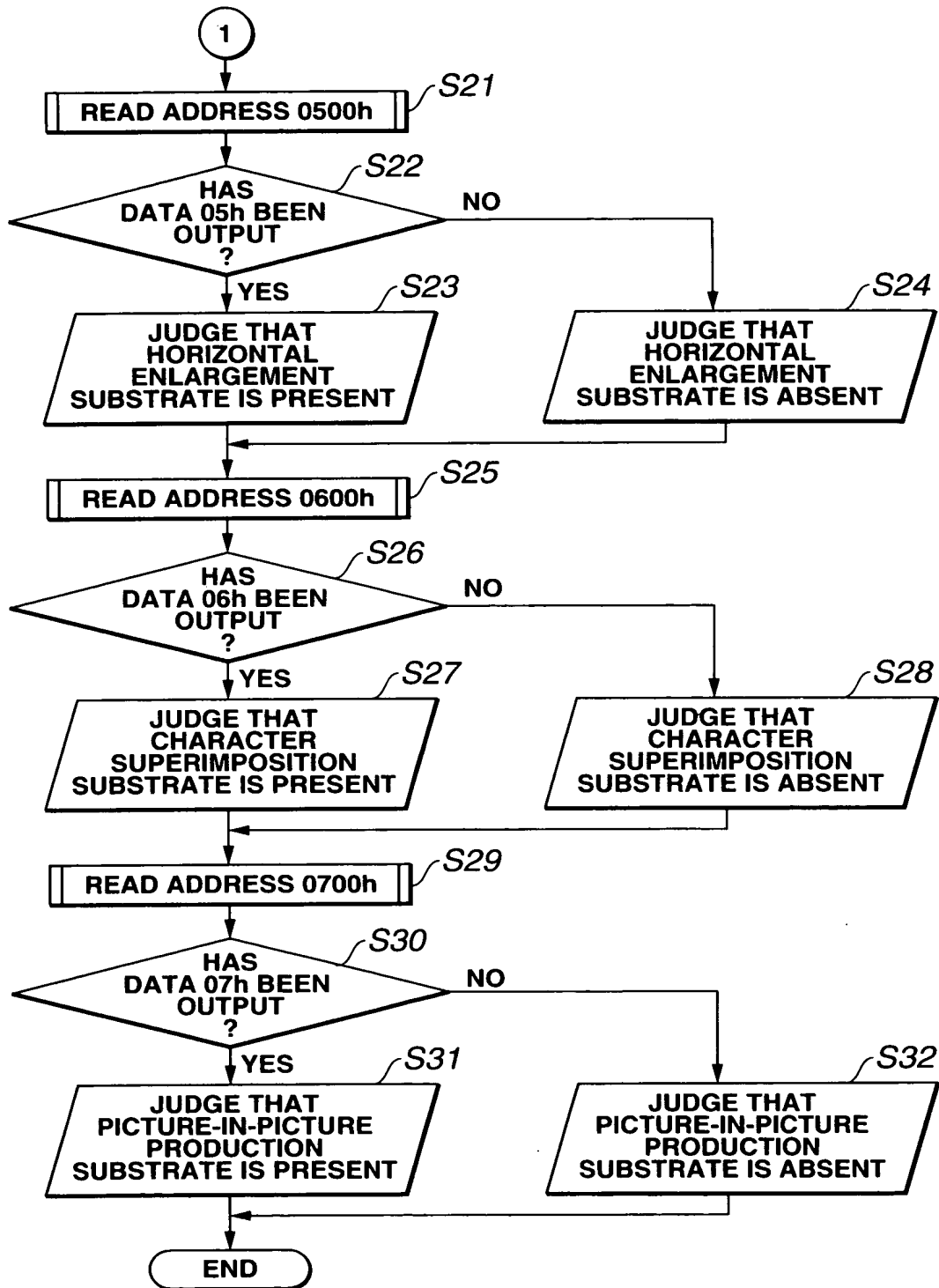
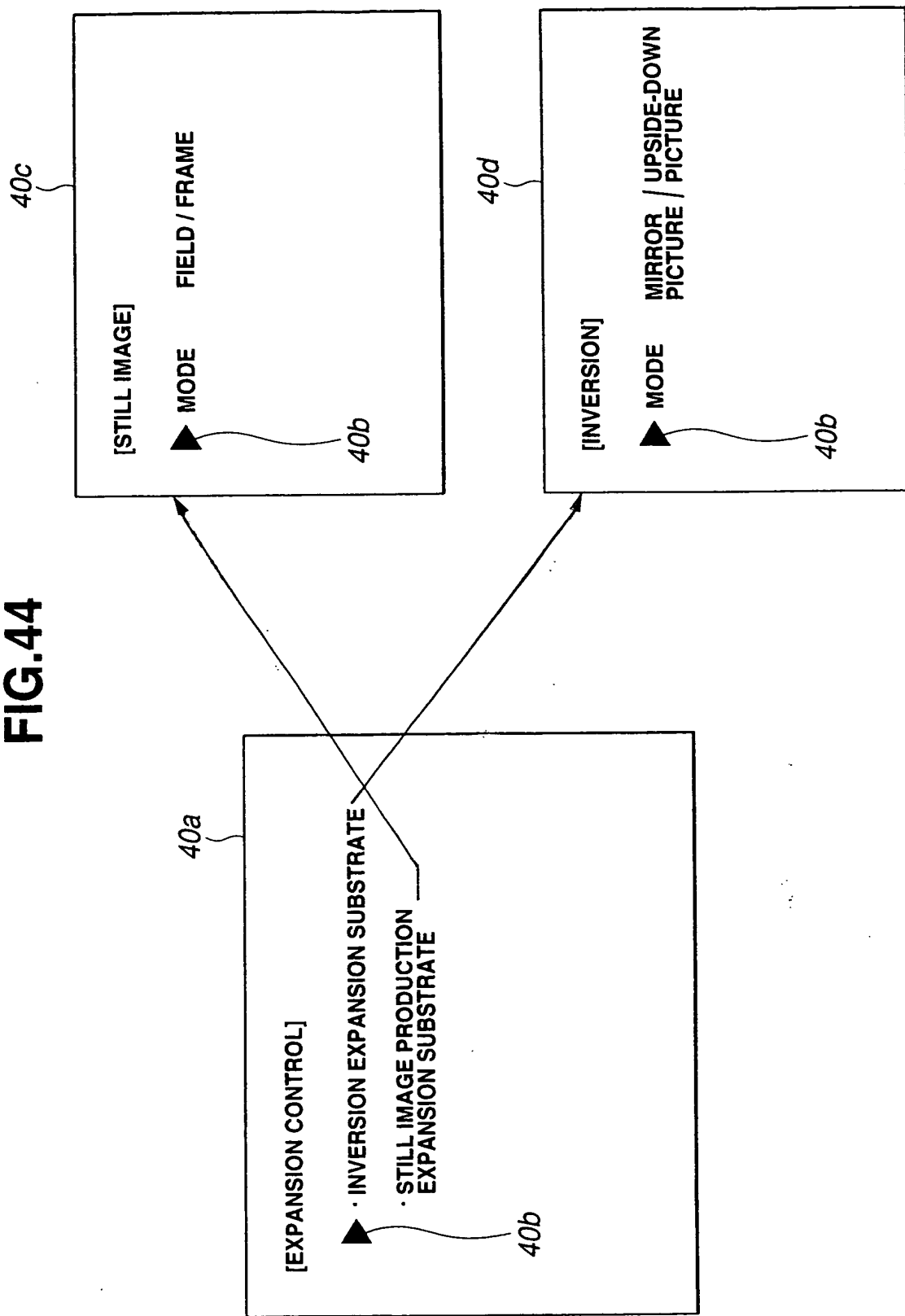


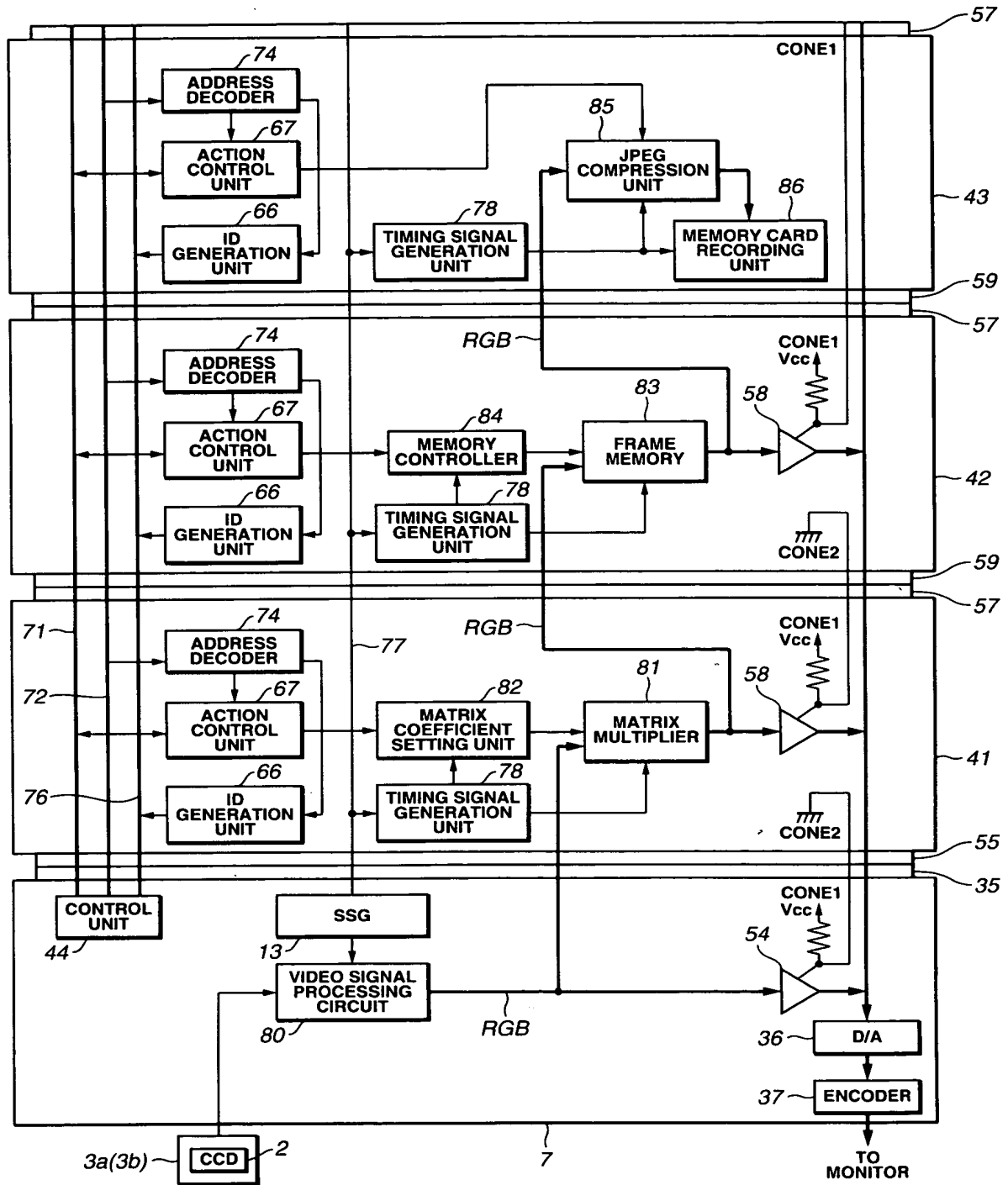
FIG.43



**FIG.44**

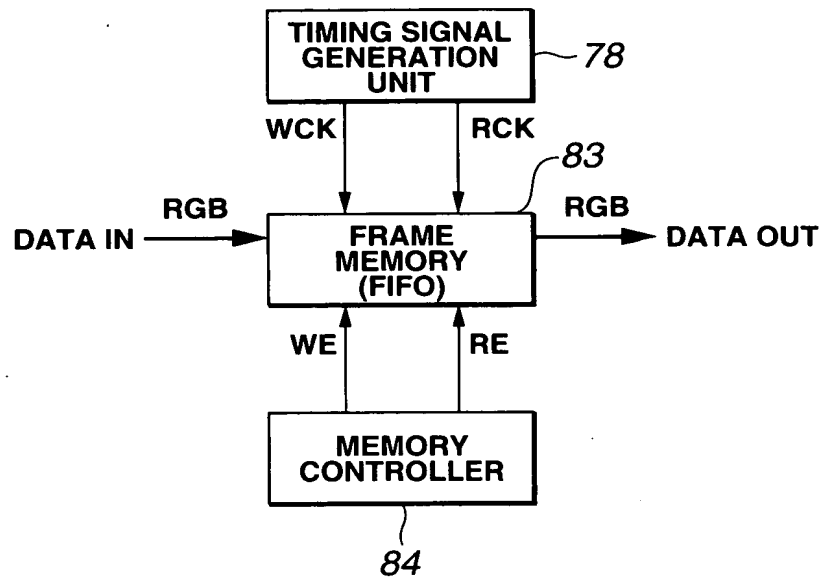


# FIG.45





**FIG.46**



**FIG.47**

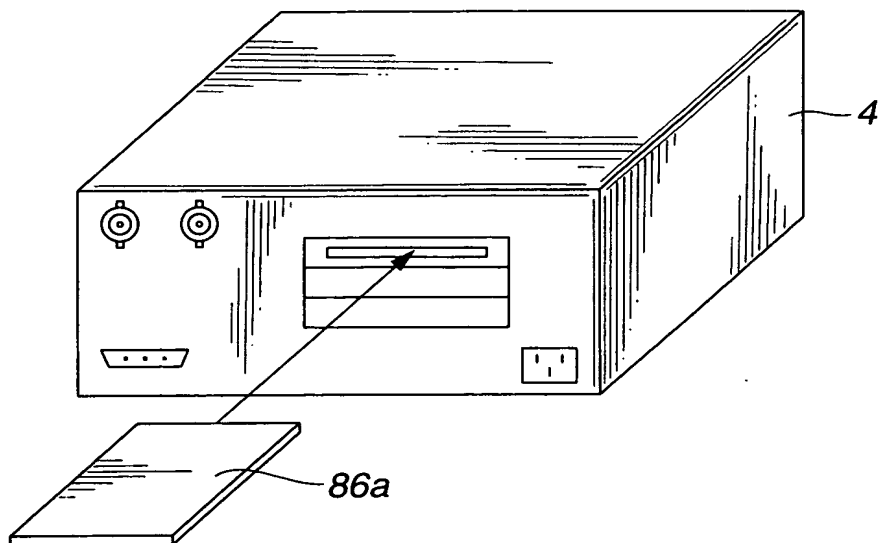
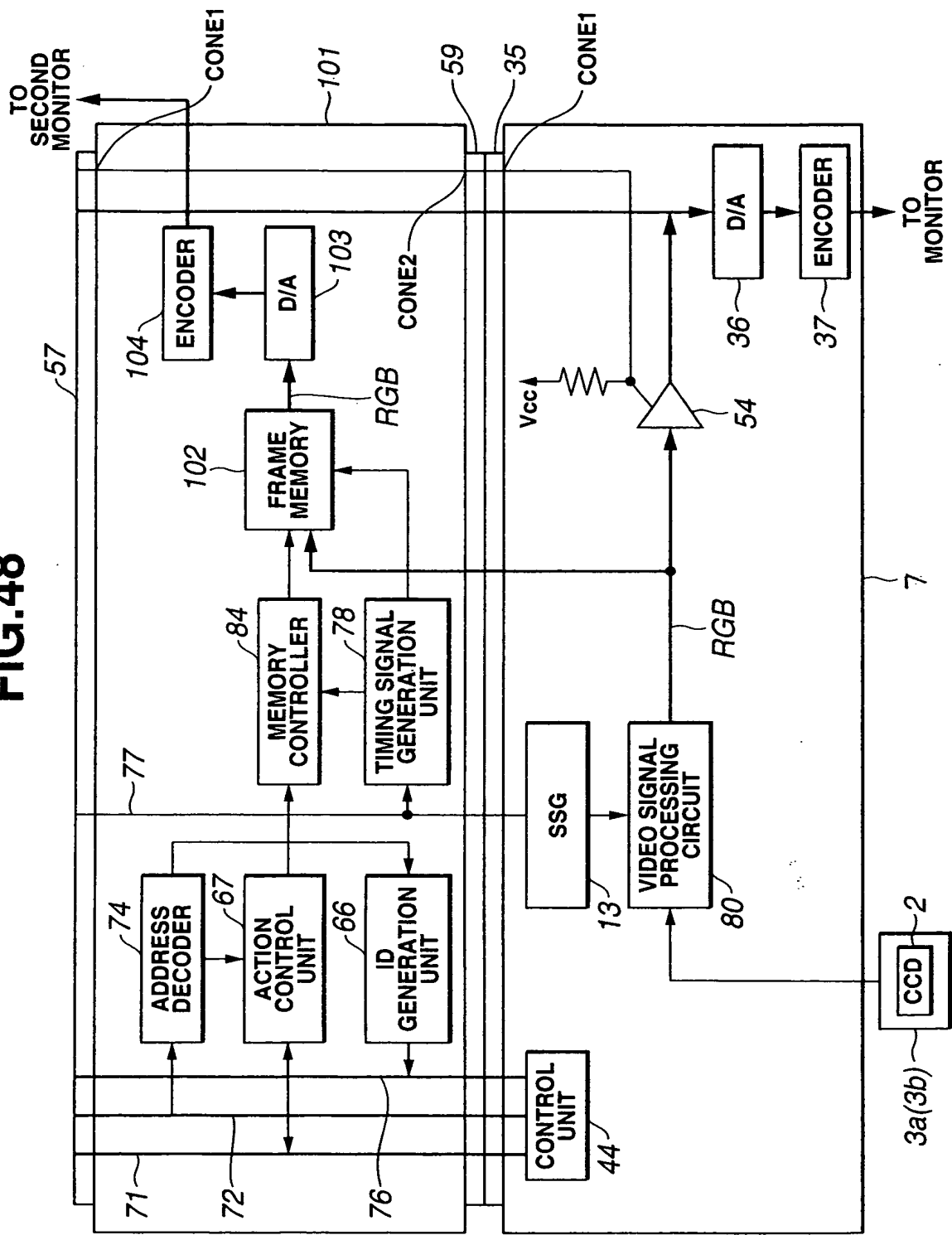
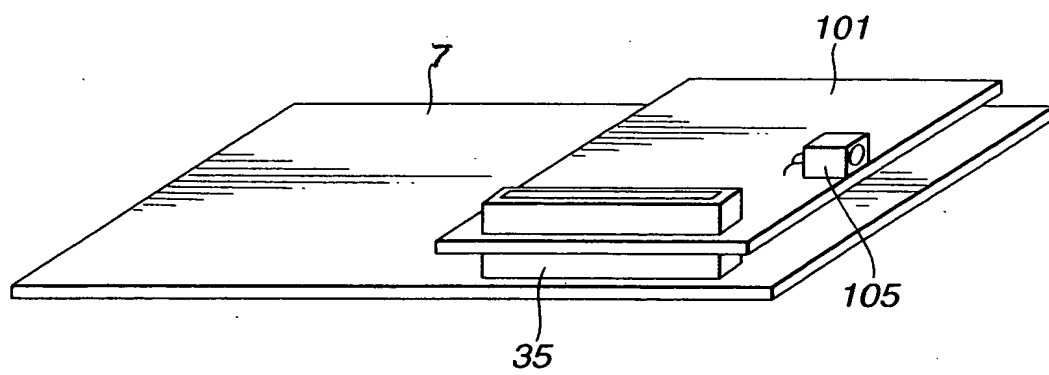


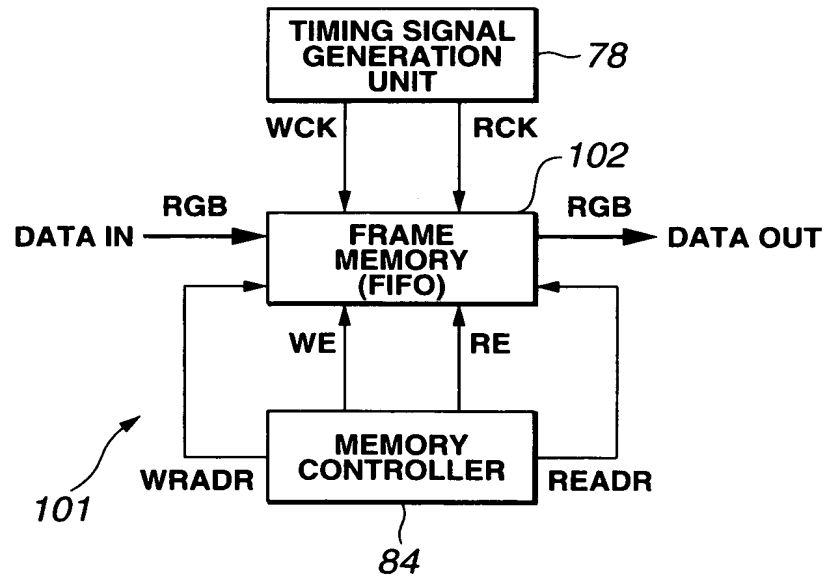
FIG.48



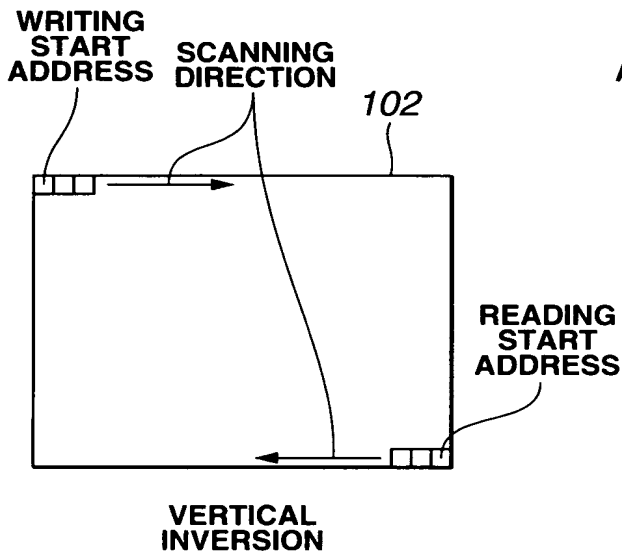
**FIG.49**



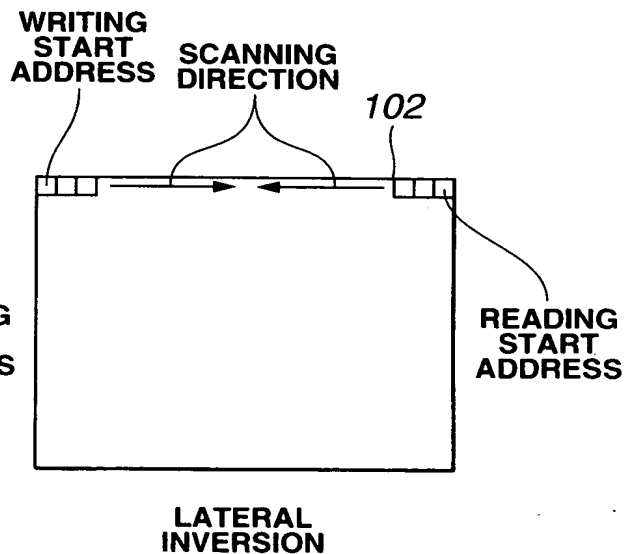
# FIG.50



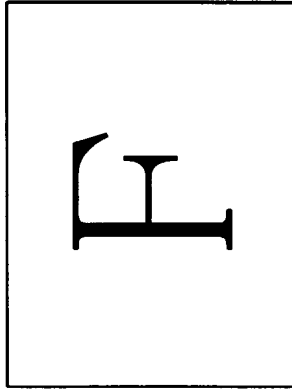
# FIG.51A



# FIG.51B

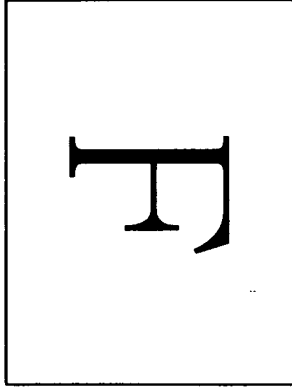


**FIG.52A**



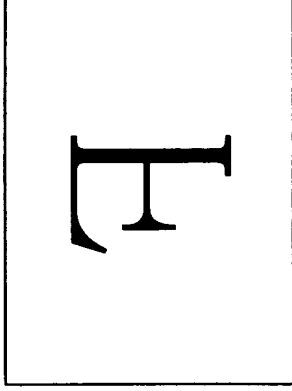
**NORMAL**

**FIG.52B**



**VERTICAL INVERSION  
(UPSIDE-DOWN)**

**FIG.52C**



**LATERAL INVERSION  
(MIRROR-IMAGE FORM)**

FIG.53

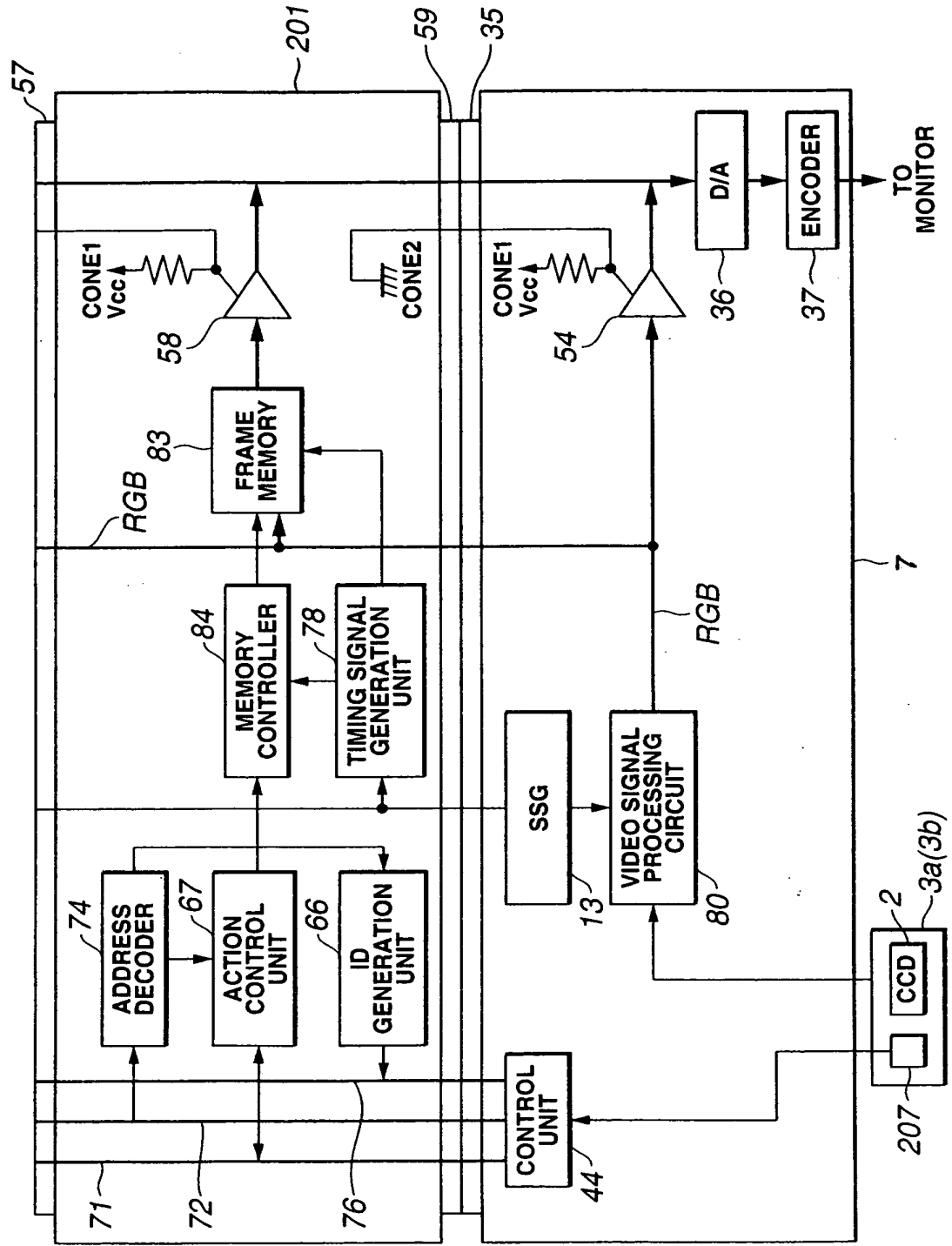


FIG.54A

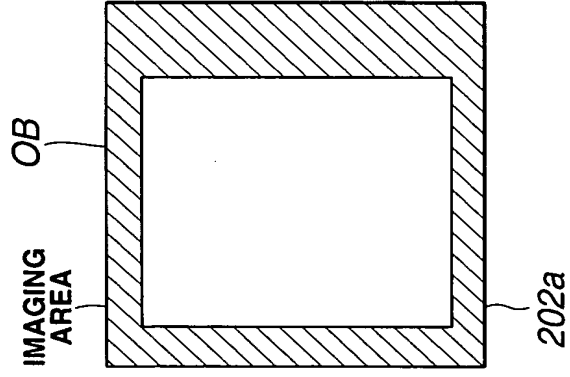


FIG.54B

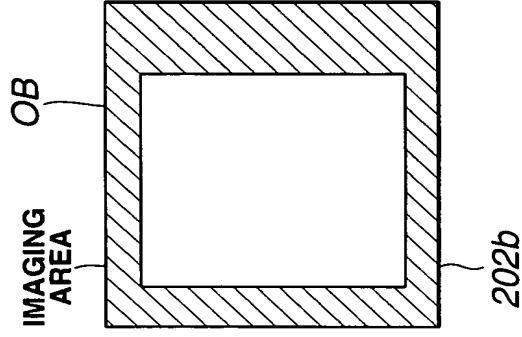
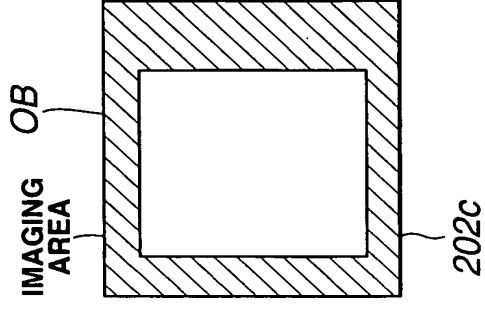
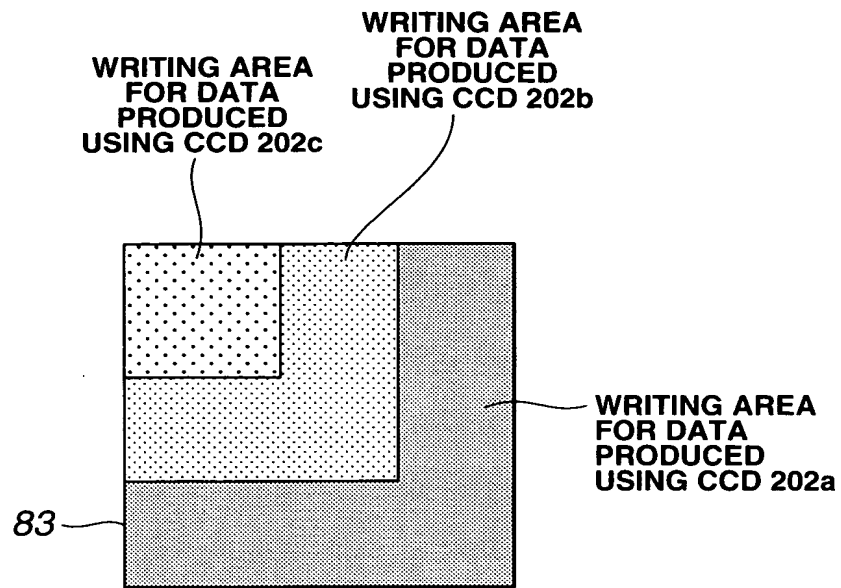


FIG.54C



**FIG.55**



**FIG.56**

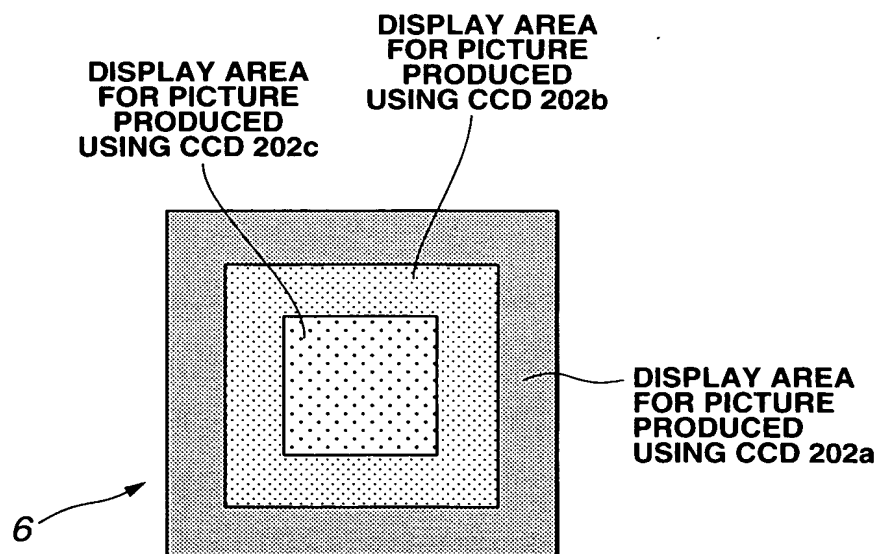
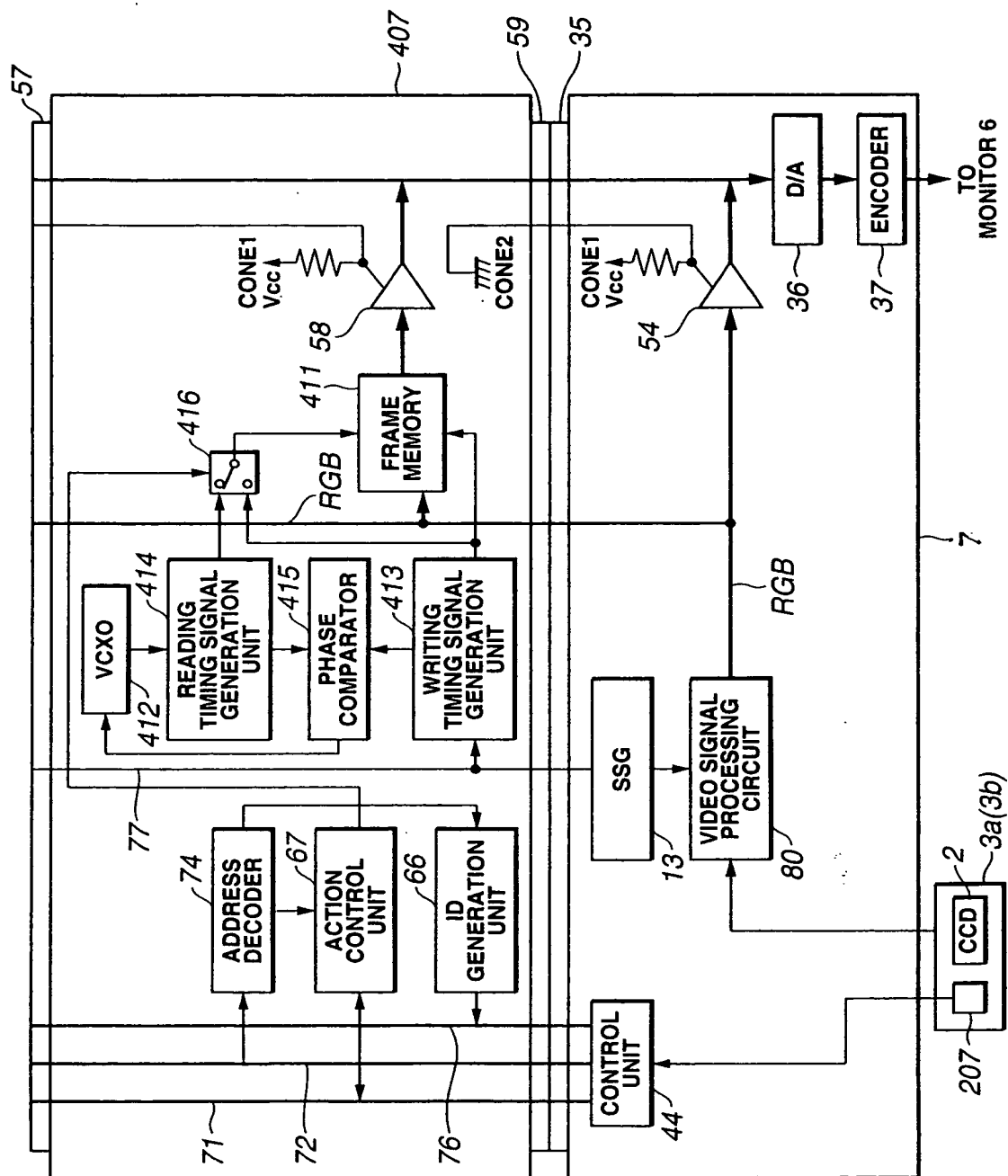
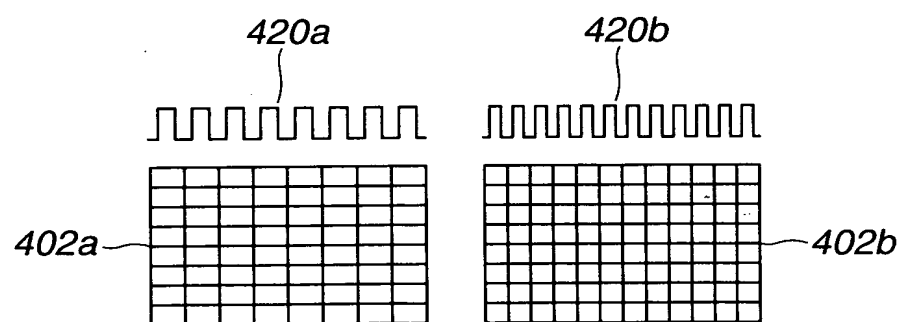




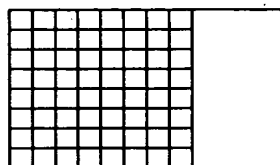
FIG.57



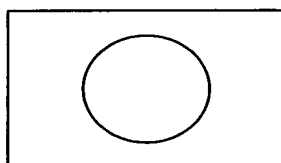
**FIG.58**



**FIG.59**



**FIG.60A**



**FIG.60B**

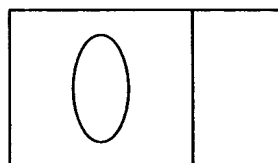


FIG. 61

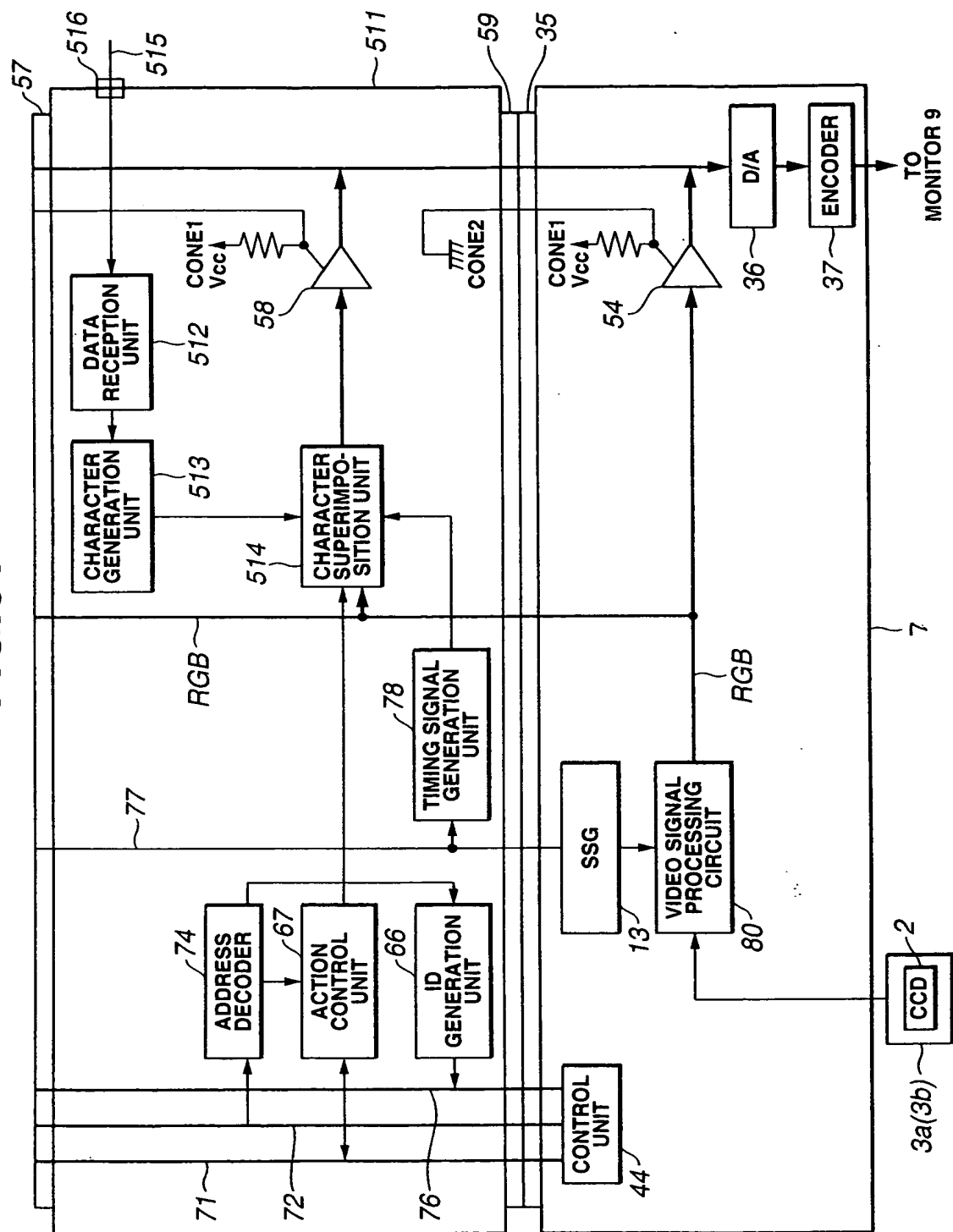
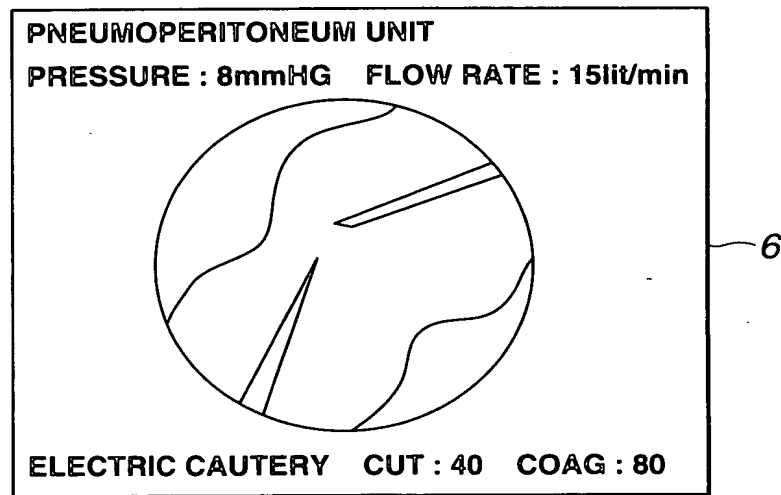


FIG.62



# FIG. 63

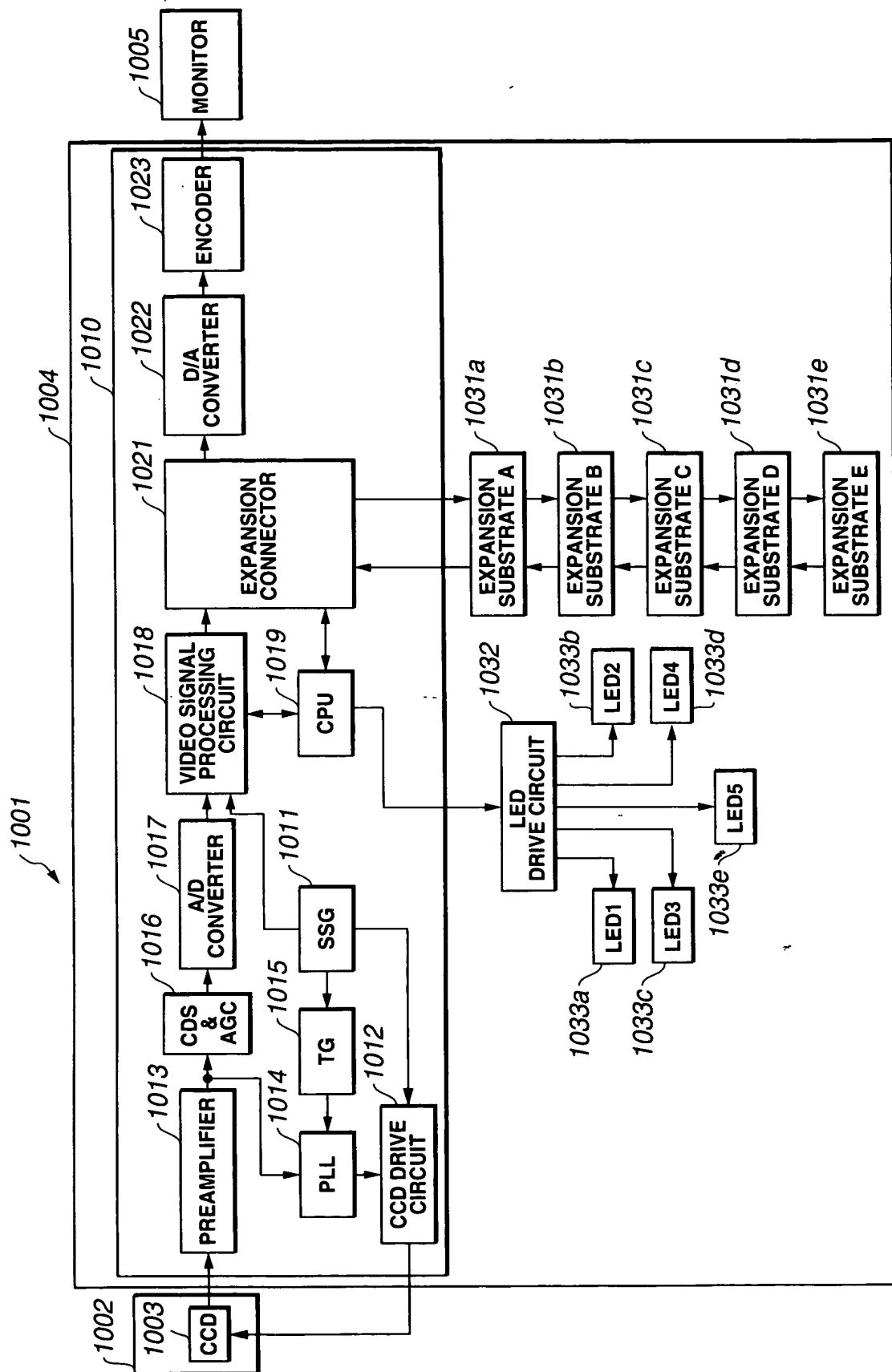
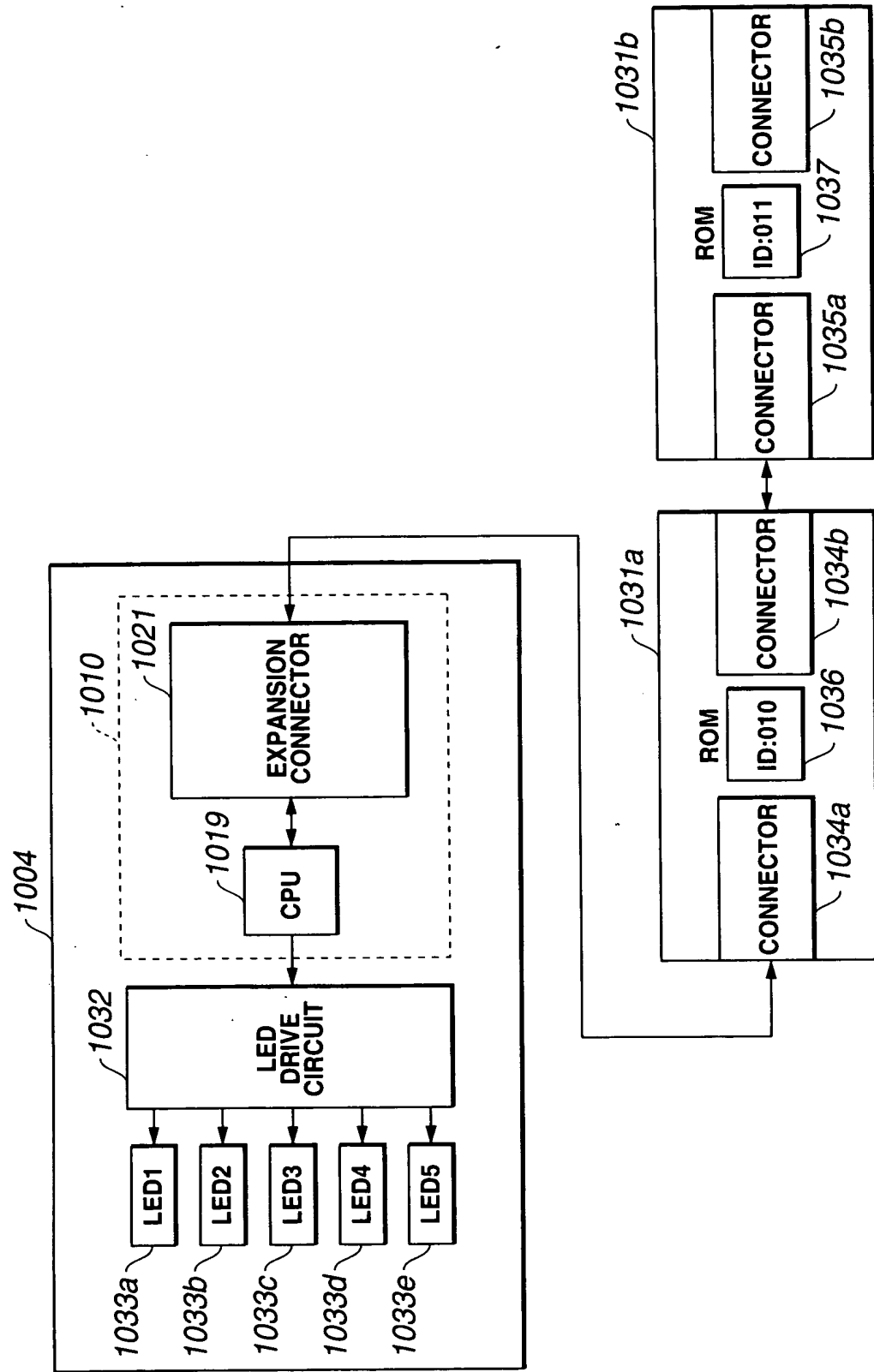
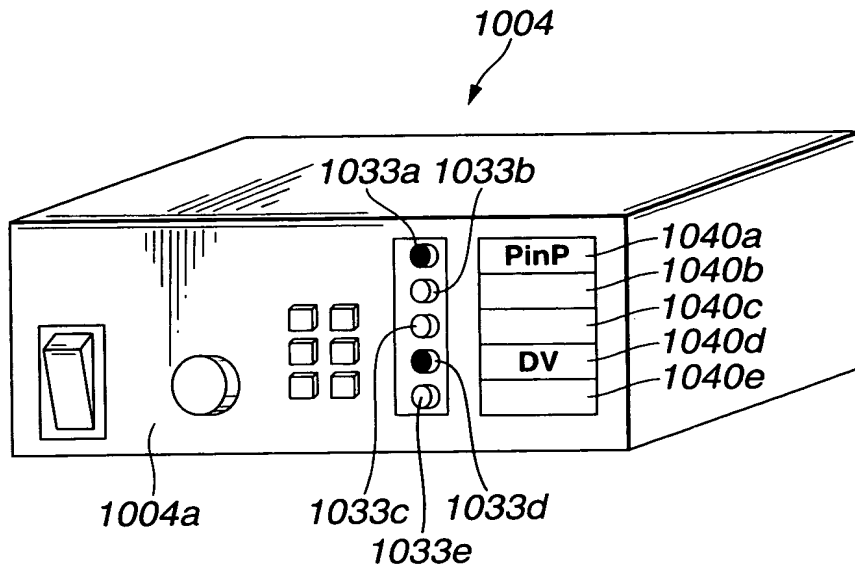


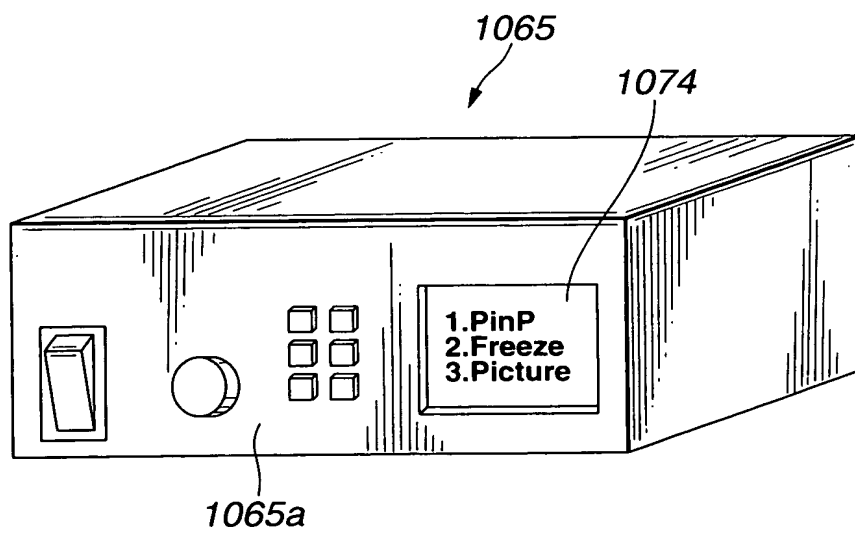
FIG. 64



**FIG.65**

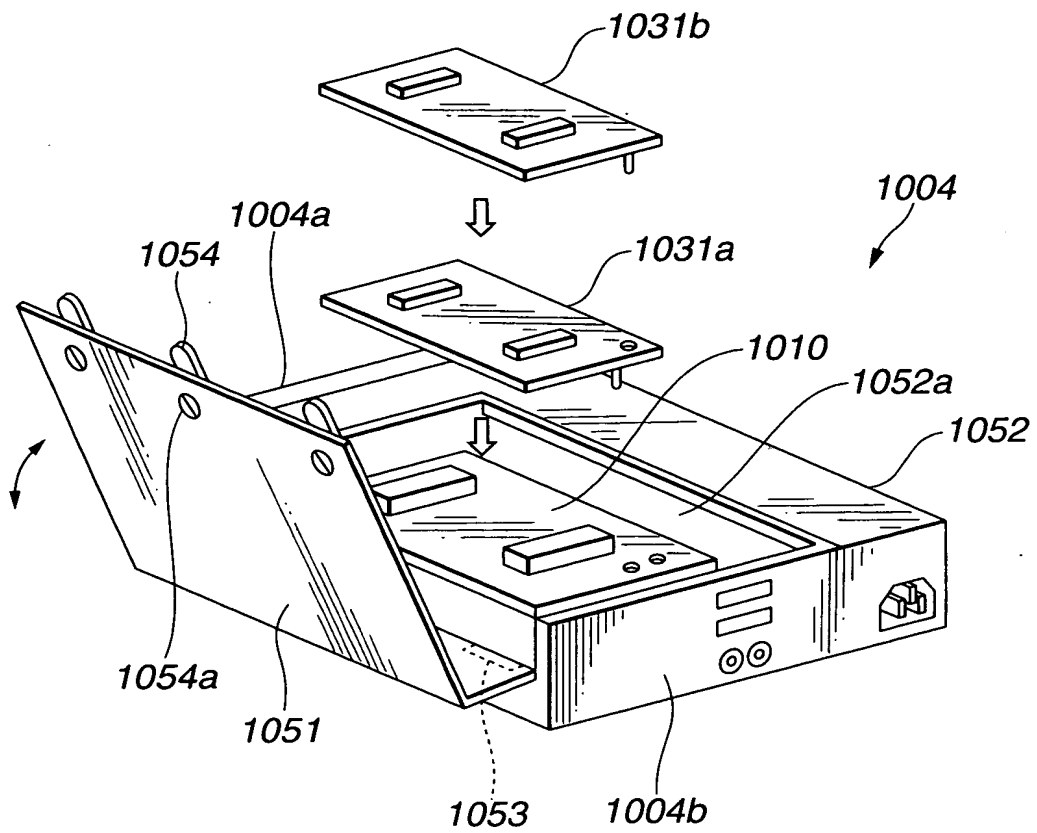


**FIG.72**

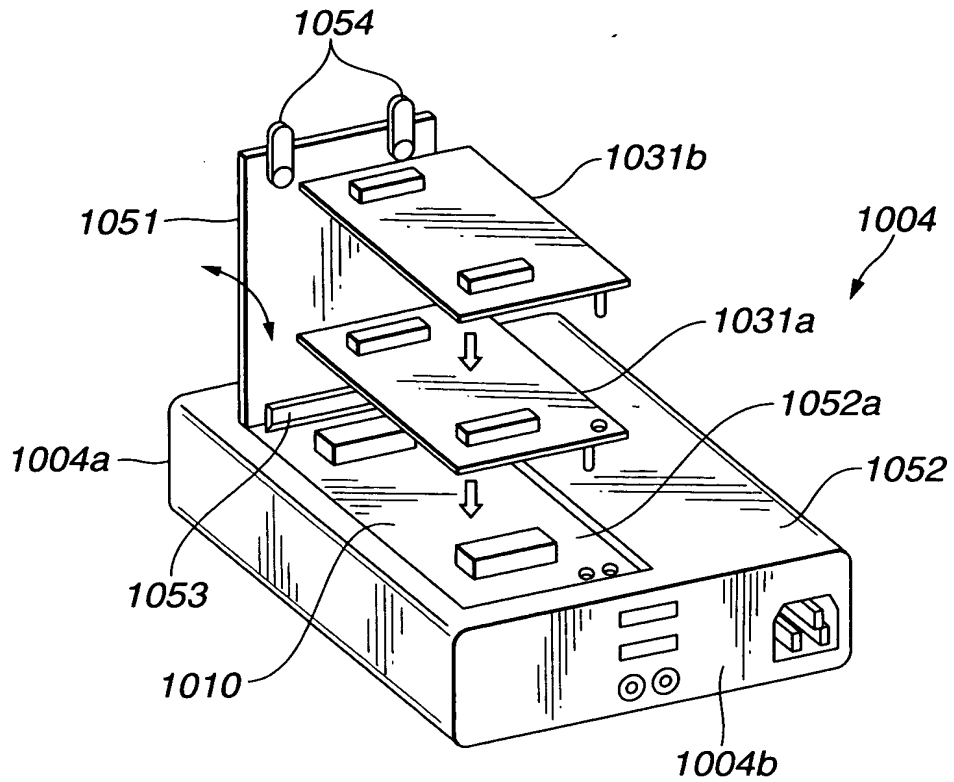




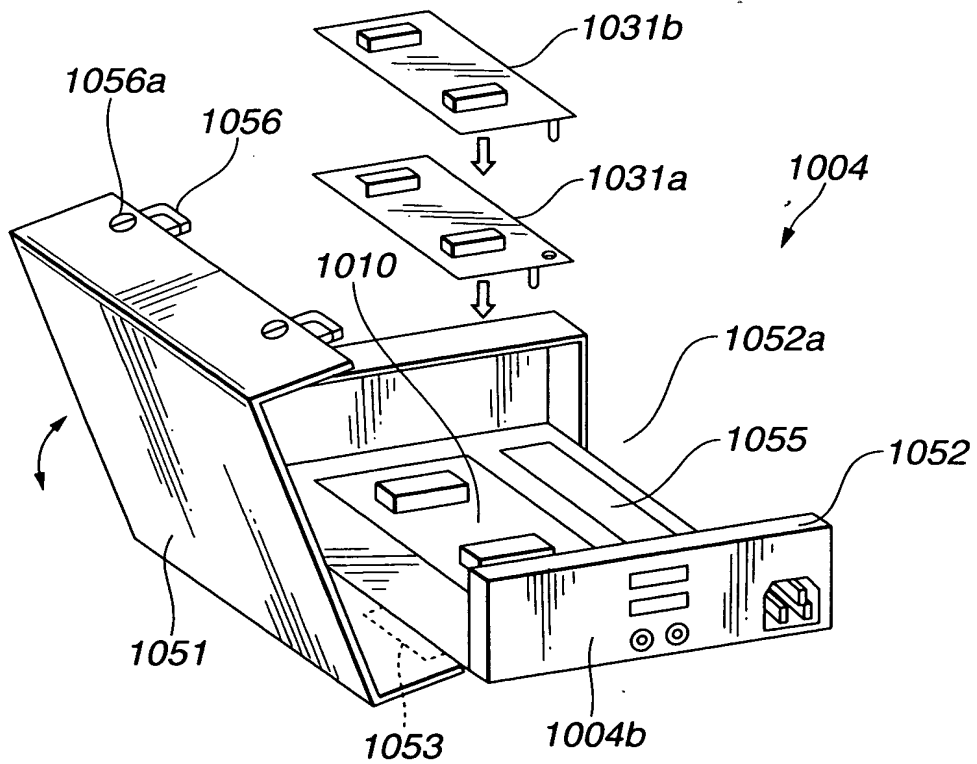
**FIG.66**



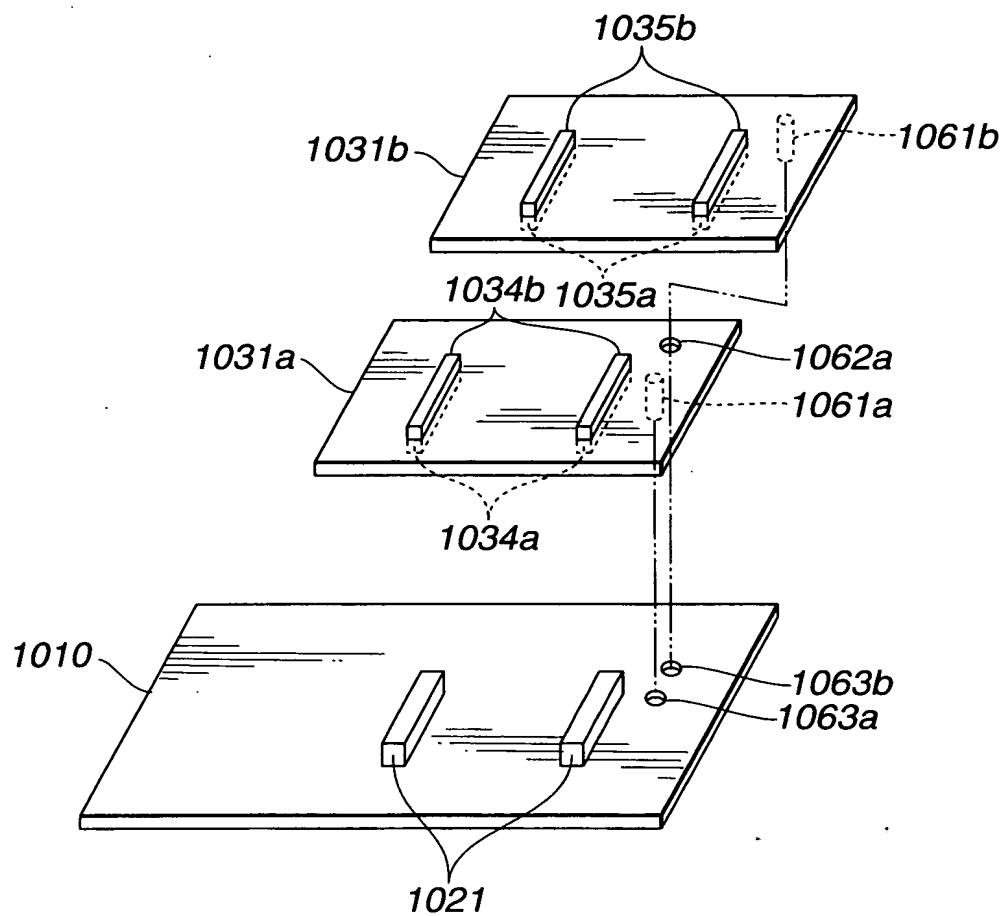
**FIG.67**



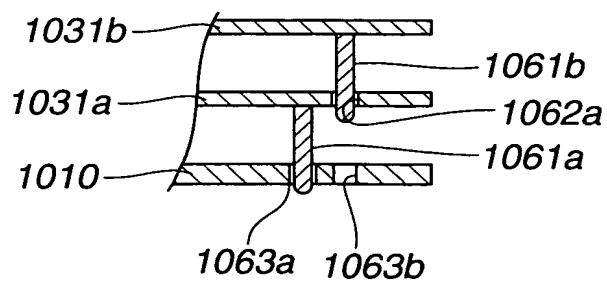
**FIG.68**



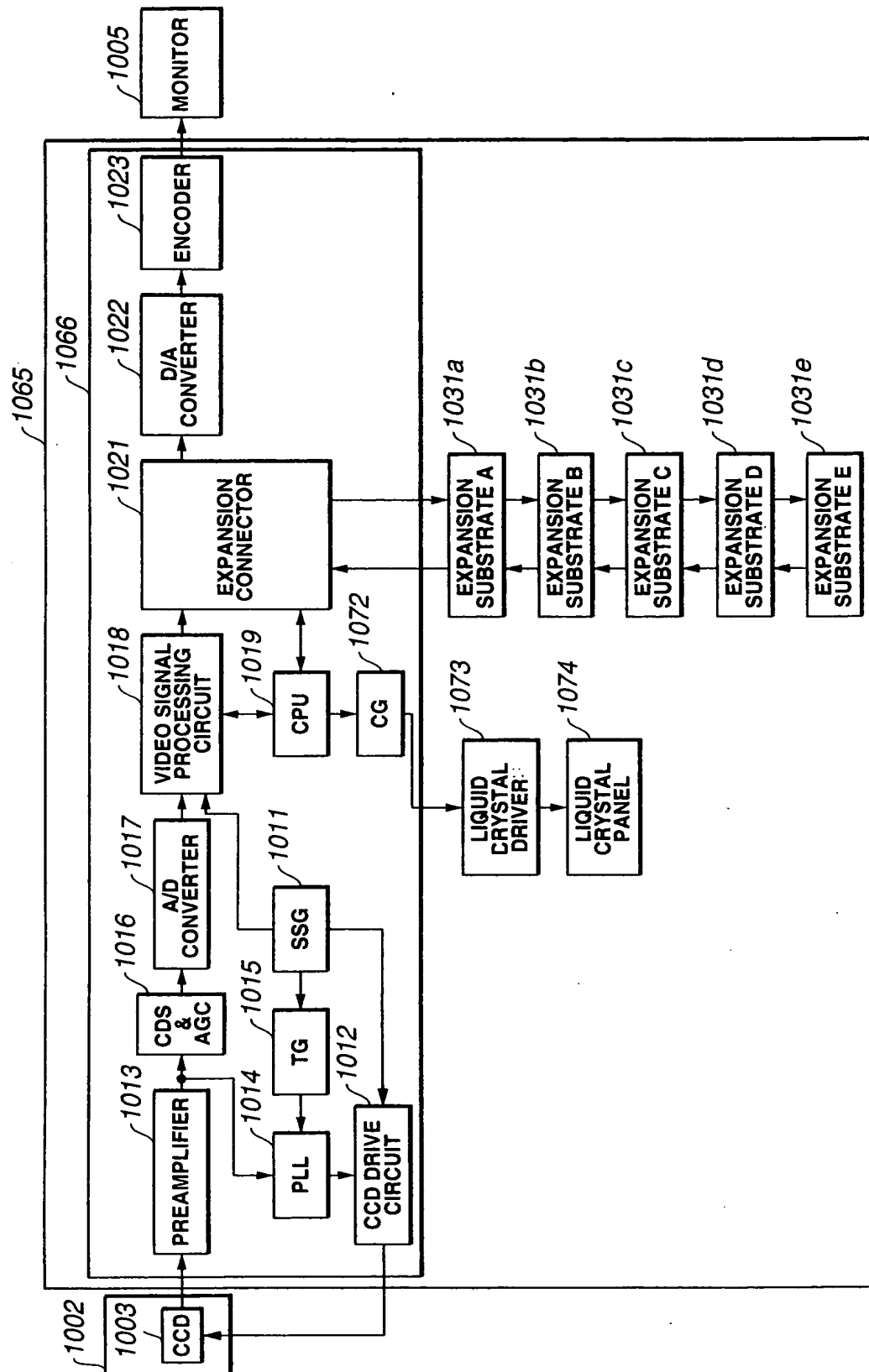
# FIG.69



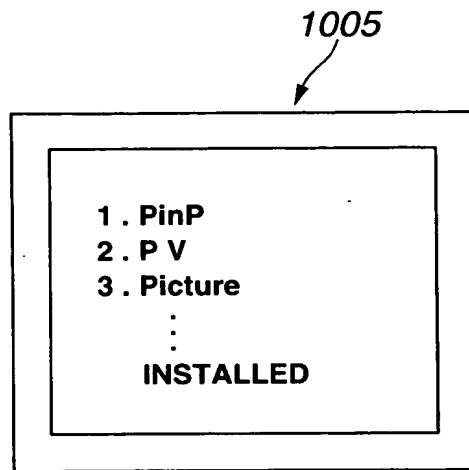
# FIG.70



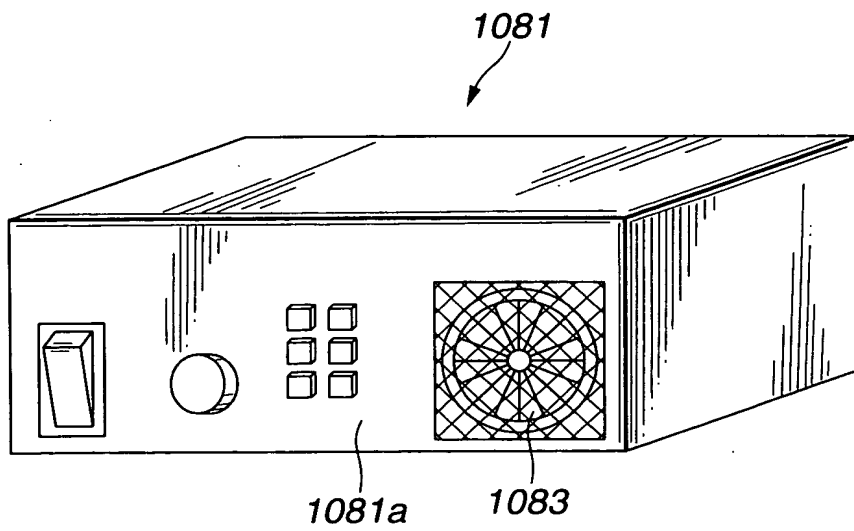
# FIG.71



**FIG.73**



**FIG.75**



**FIG. 74**

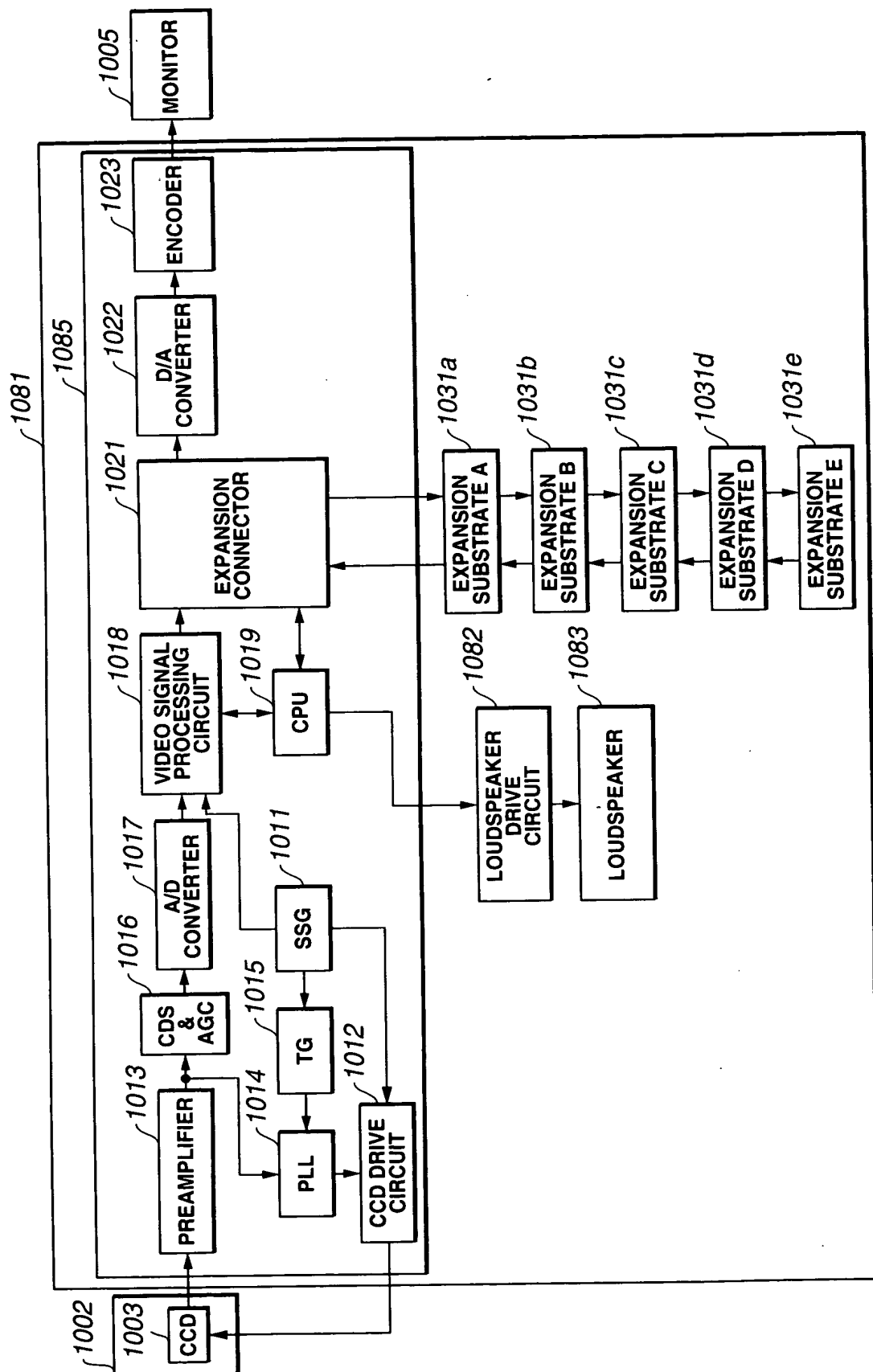
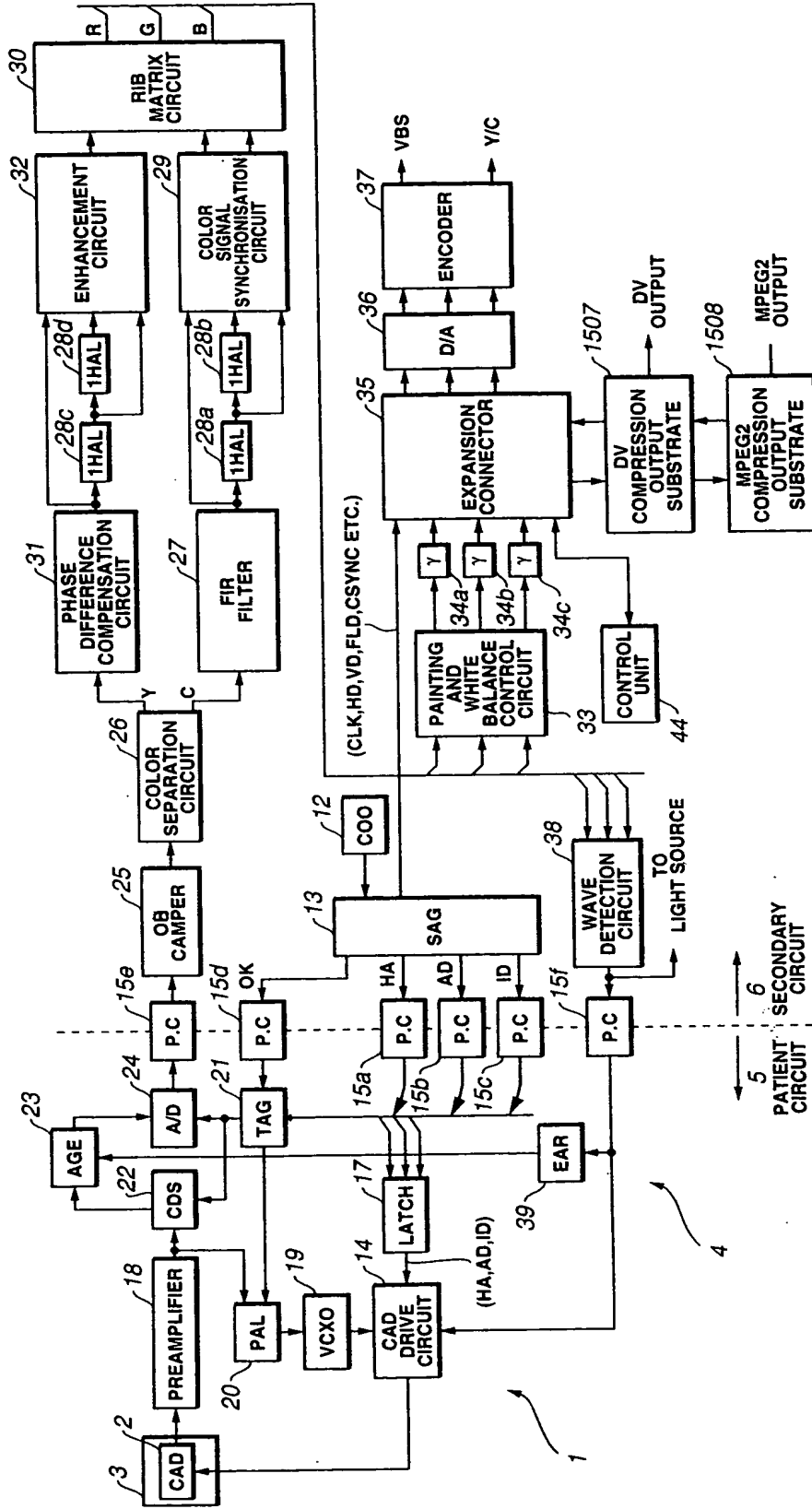
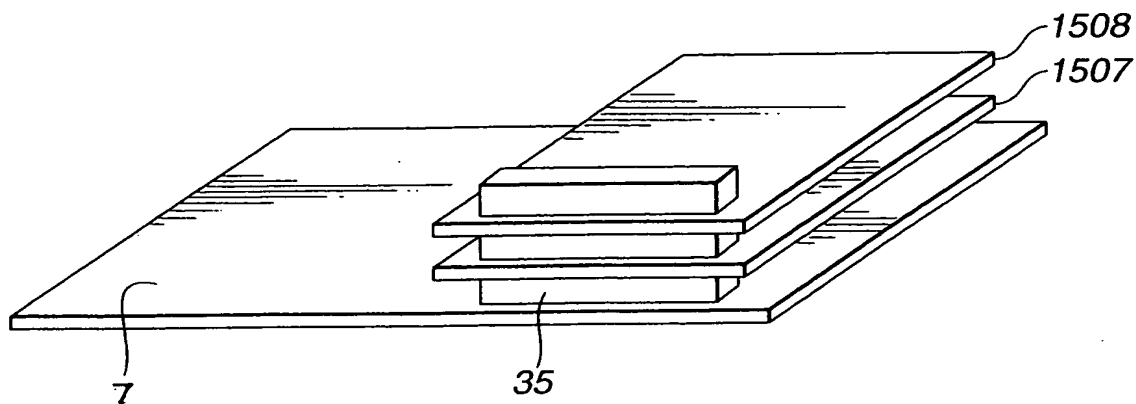


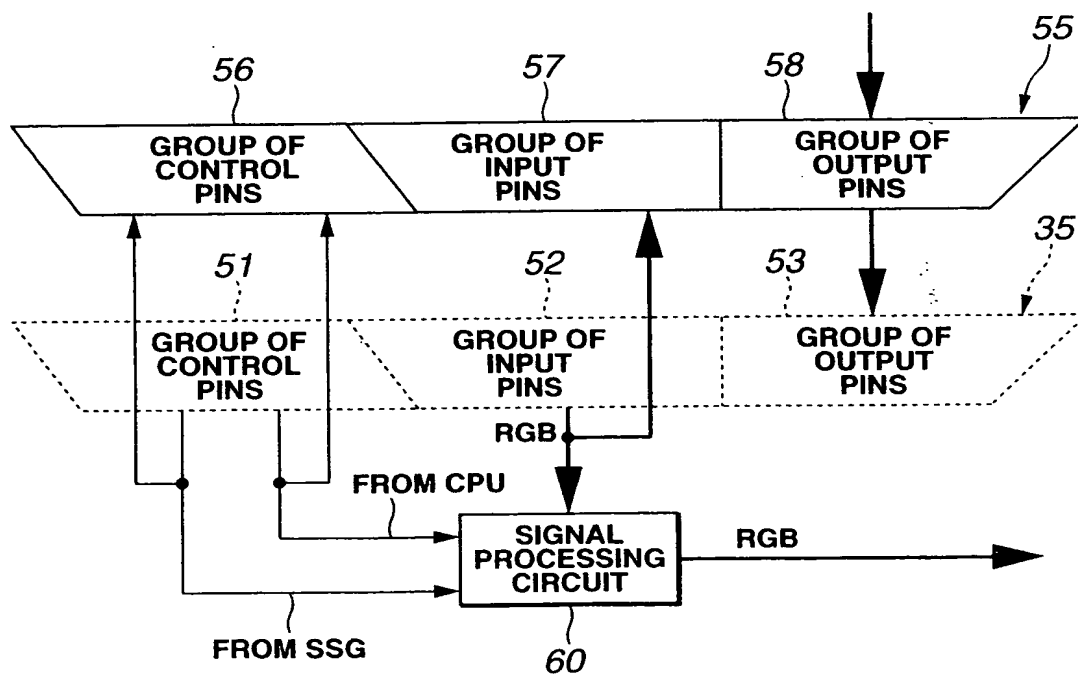
FIG.76



**FIG.77**

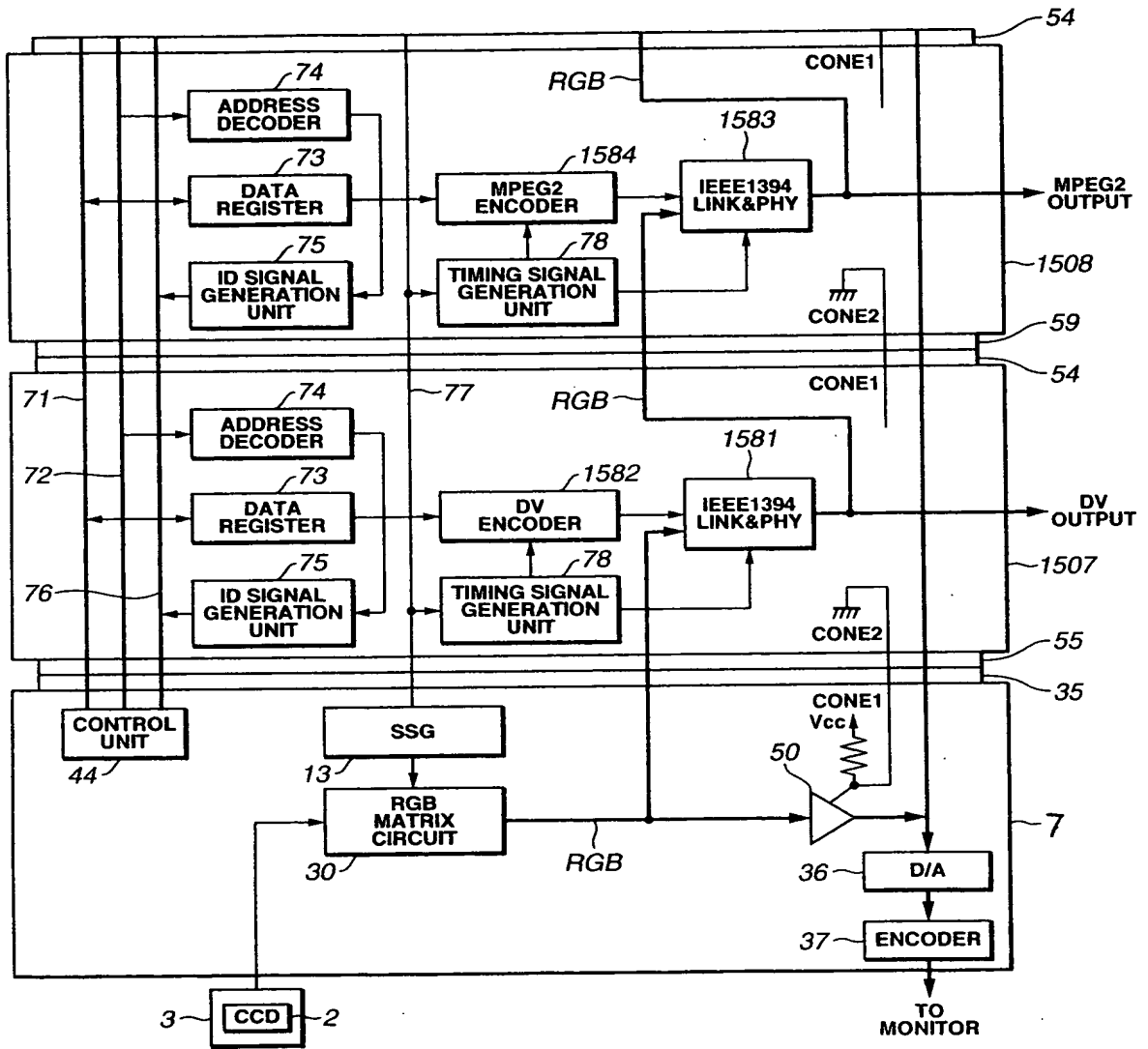


**FIG.79**





# FIG.78



**FIG.80**

